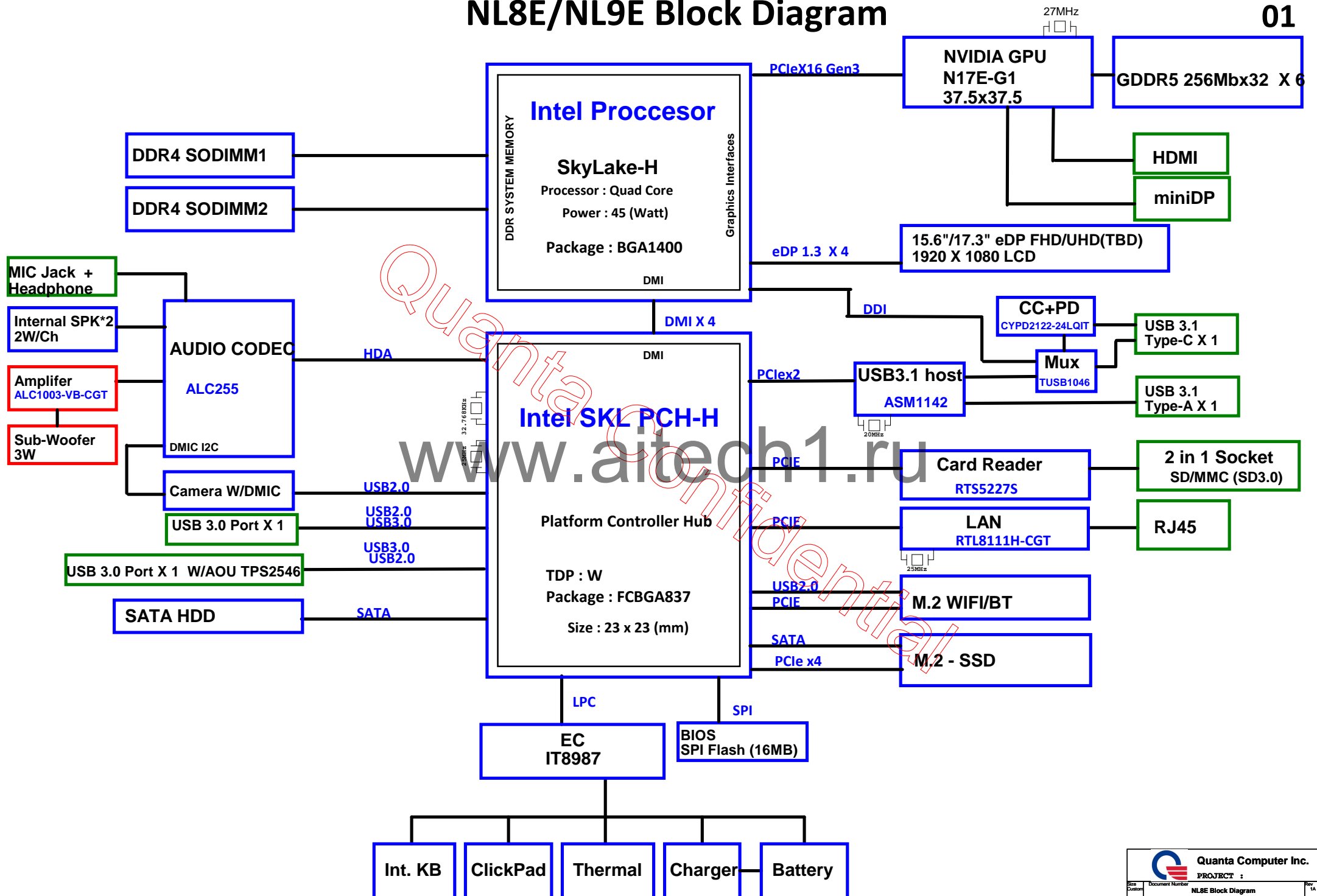






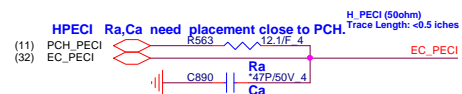


NL8E/NL9E Block Diagram

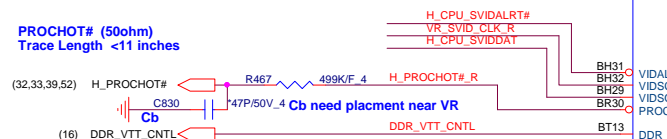
01



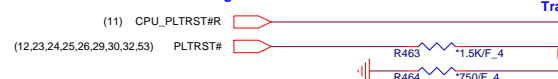
(11)	CLK_CPU_BCLKP		CLK_CPU_BCLKP	B31	BCLK
(11)	CLK_CPU_BCLKN		CLK_CPU_BCLKN	A32	
(11)	CPU_PCI_BCLKP		CPU_PCI_BCLKP	D35	PCI_E
(11)	CPU_PCI_BCLKN		CPU_PCI_BCLKN	C36	
(11)	CLK_DPLL_NSCCLKP		CLK_DPLL_NSCCLKP	E31	CLK2
(11)	CLK_DPLL_NSCCLKN		CLK_DPLL_NSCCLKN	D31	



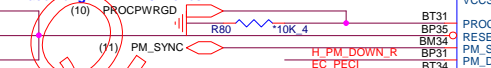
PROCHOT# (50ohm)
Trace Length <11 inches



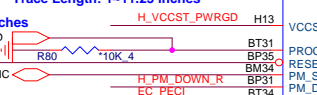
CPU RESET# CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



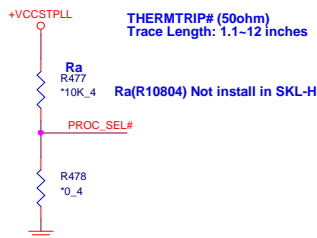
PM_SYNC (50ohm)
Trace Length: 1~11.25 inches



PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches



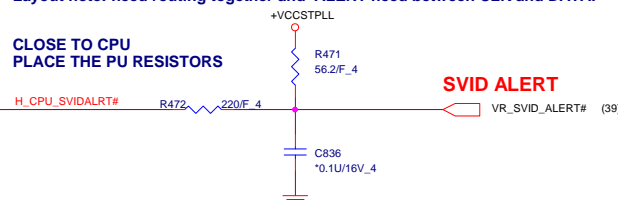
THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches



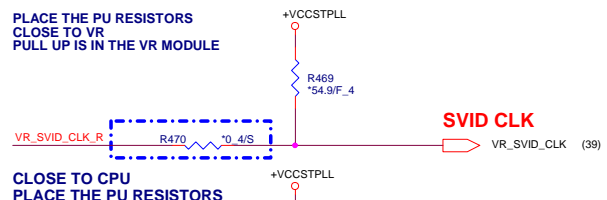
CPU CORE SVID

Layout note: need routing together and ALERT need between CLK and DATA.

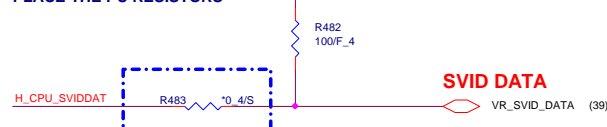
**CLOSE TO CPU
PLACE THE PU RESISTORS**



PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



**CLOSE TO CPU
PLACE THE PU RESISTORS**








VW

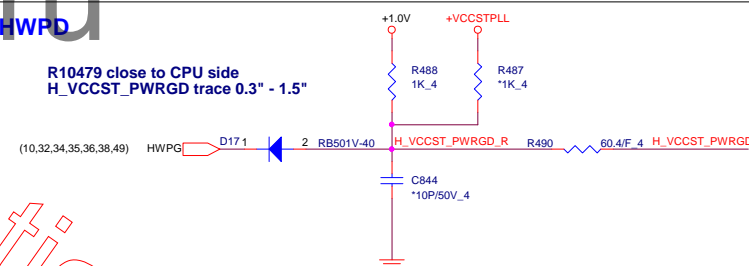
HWPD

0 Enable: SET DFX ENABLED BIT IN DEBUG

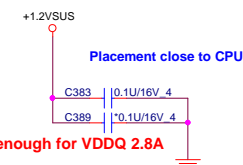
1 , Disable;



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a O&M board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R88  1K 4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R491  1K 4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved	CFG6 R493  *1K 4
		x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG5 R492  *1K 4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training	CFG7 R489  *1K 4



CPU VDDQ



Note: please keep plane is enough for VDDQ 2.8A



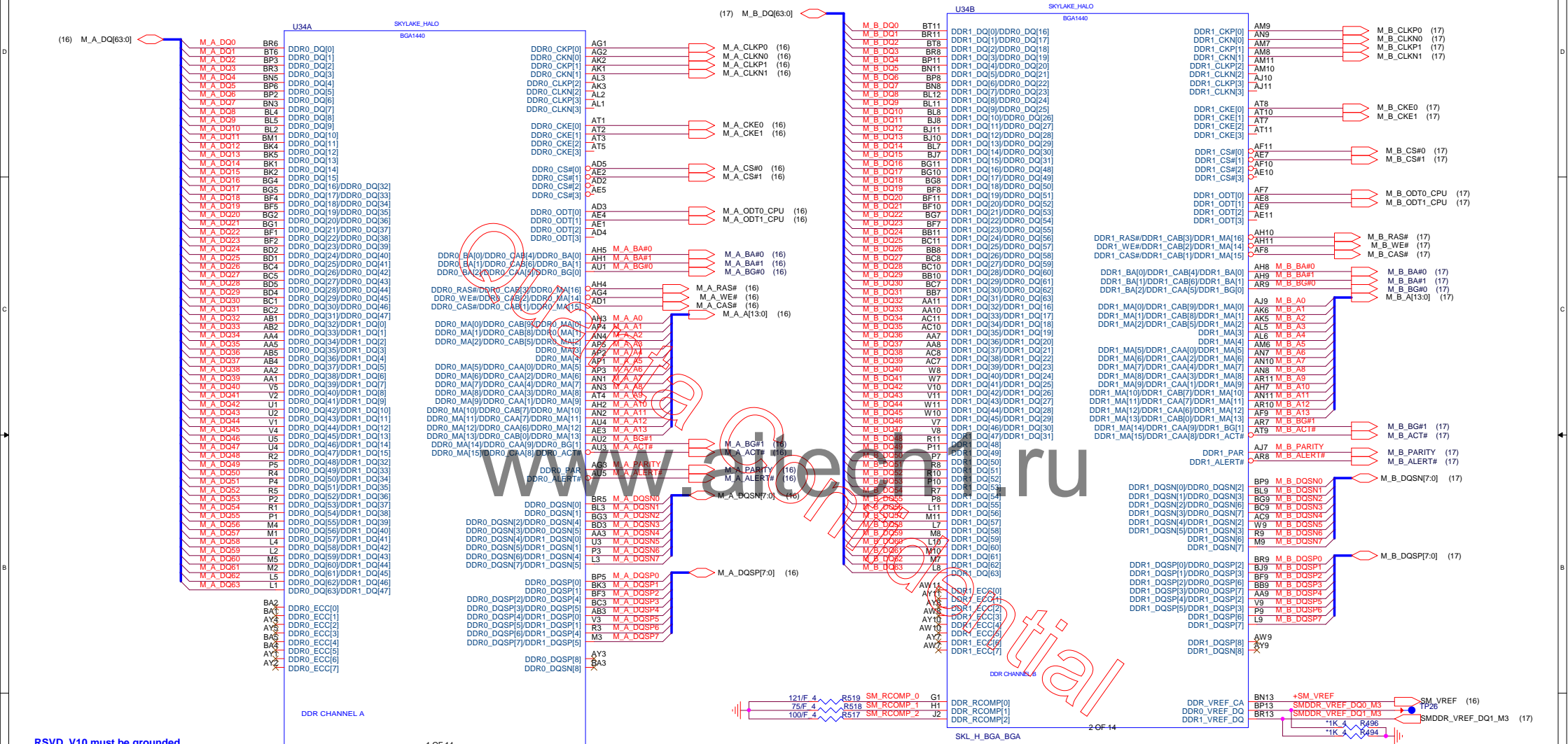
Quanta Computer Inc.

PROJECT :

Size	Document Number Custom	02 – SKYPAKE 1/20(eDP/DDI)	Rev 1A
Date:	Thursday, August 25, 2016	Sheet 2 of	68



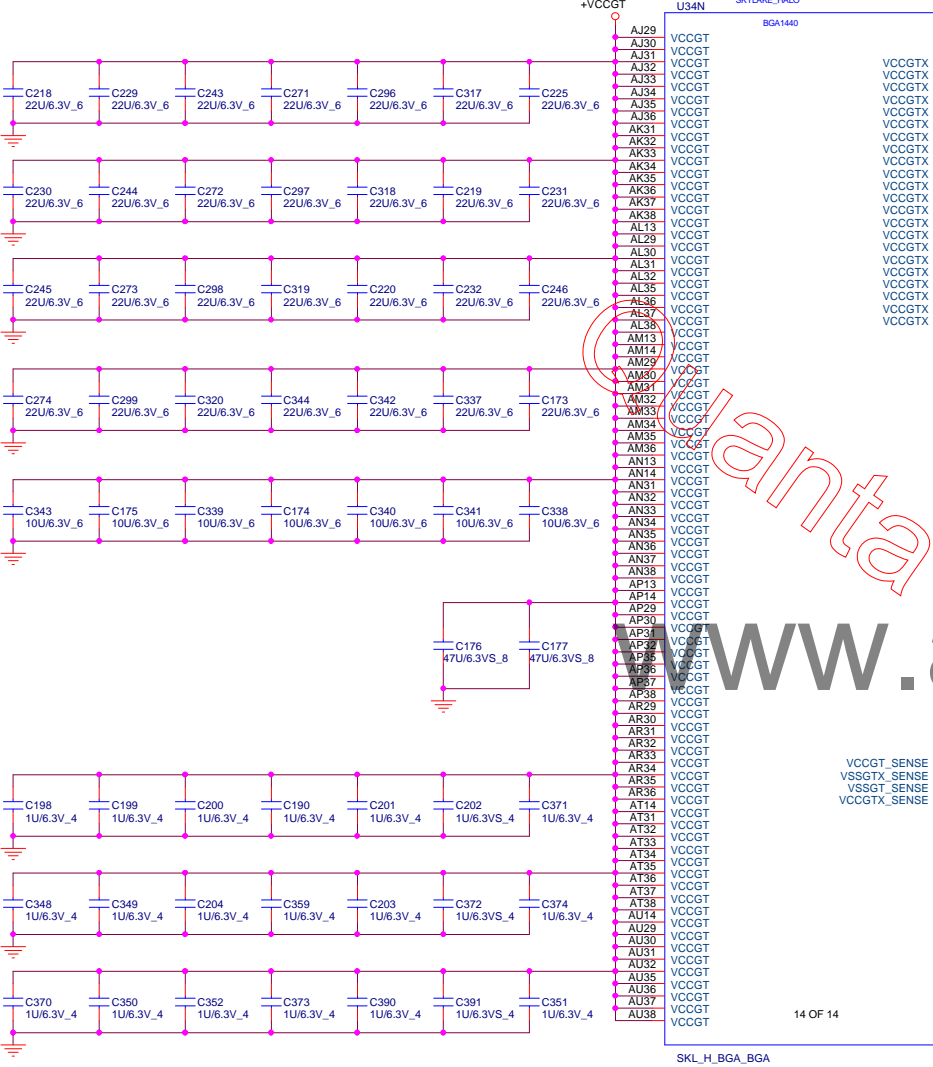
SKYLAKE Processor (DDR4)



Follow SKL H EDS page 133 to 45W(GT4+OPC): +VCCGT=104A/12A (GTx)
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

4+4e, Support eDRAM Only, GTX 12A

+VCC CORE (40,44,7)
+1.2VSUS (10,16,17,2,35,43,44,50,6)



AF29
AF30
AF31
AF32
AF33
AF34
AG13
AG14
AG31
AG32
AG33
AG34
AG35
AG36
AH13
AH14
AH29
AH30
AH31
AH32
AJ13
AJ14

AH38
AH35
AH37
AH36

VCCGT_SENSE (39)
VSSGT_SENSE (39)
VSSGT_SENSE (39)

14 OF 14

SKL_H_BGA_BGA

VCC Output Decoupling Recommendations

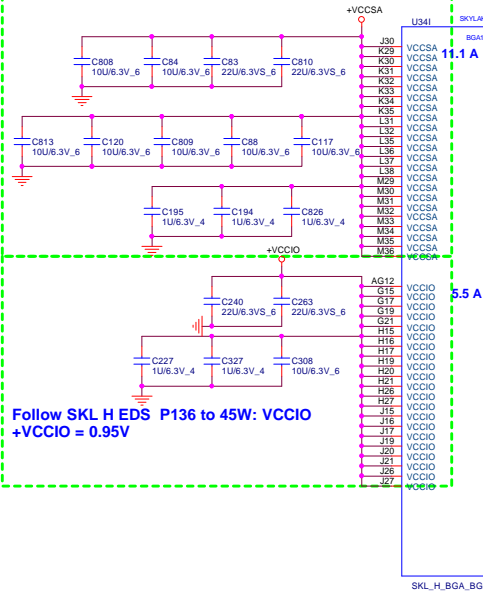


Quanta Computer Inc.

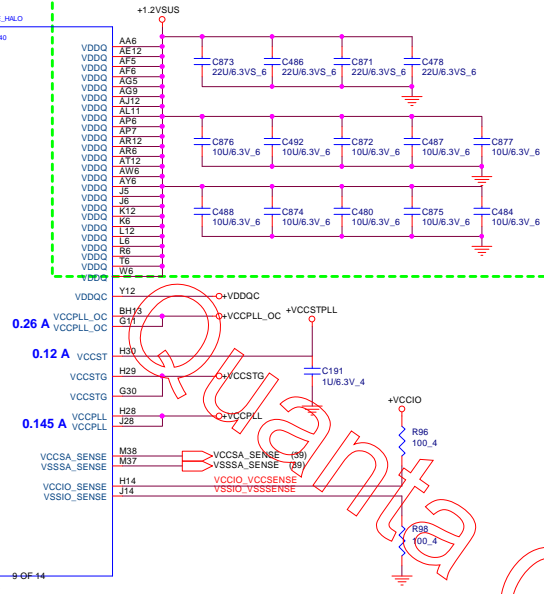
PROJECT :

Size	Document Number	Custom	SNB 3/5 (POWER)	Rev	2A
Date:	Thursday, August 25, 2016	Sheet	5	of	68

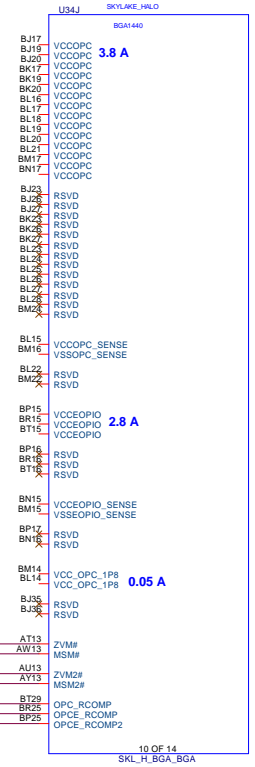
Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A (GTx)



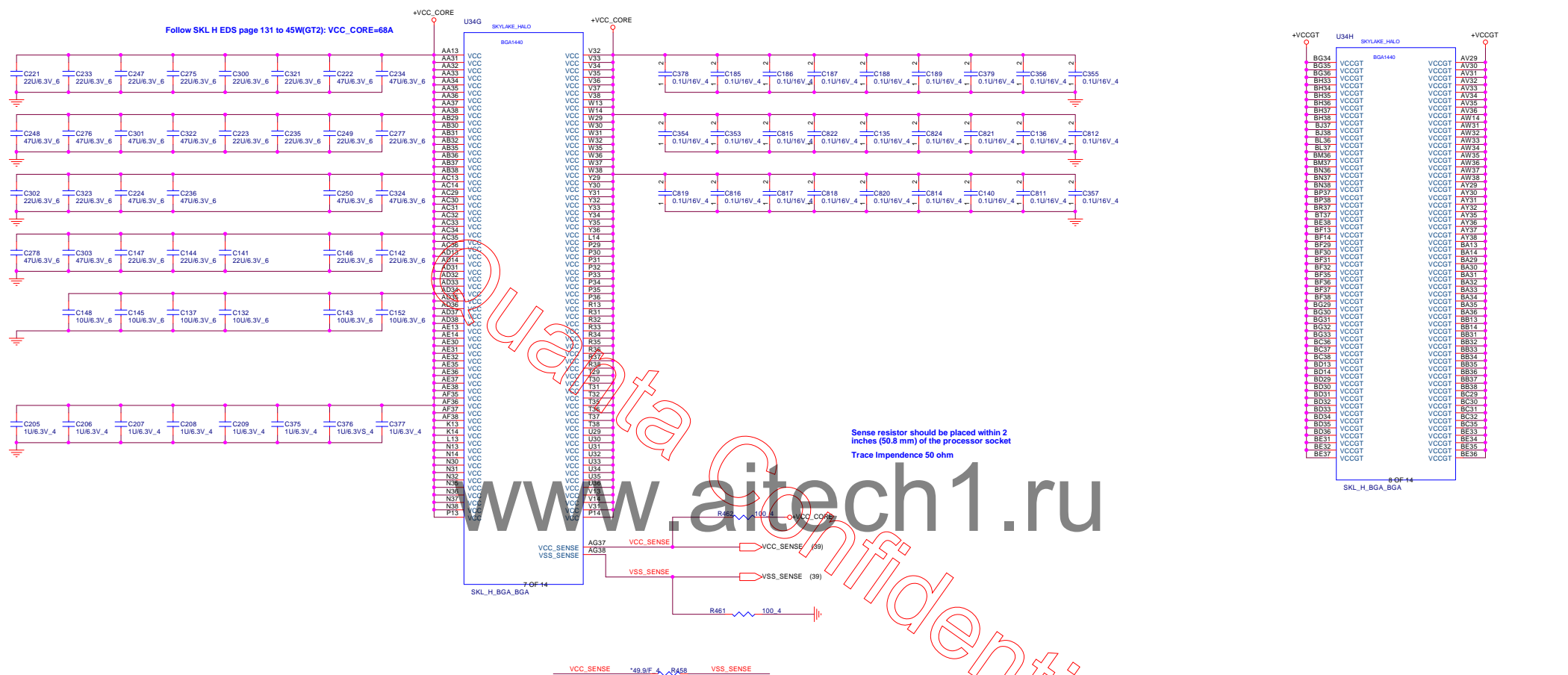
Follow SKL H EDS page 135 45W: VDDQ=2.8A



EDRAM Only, PLACE CAPS IN ACK SIDE

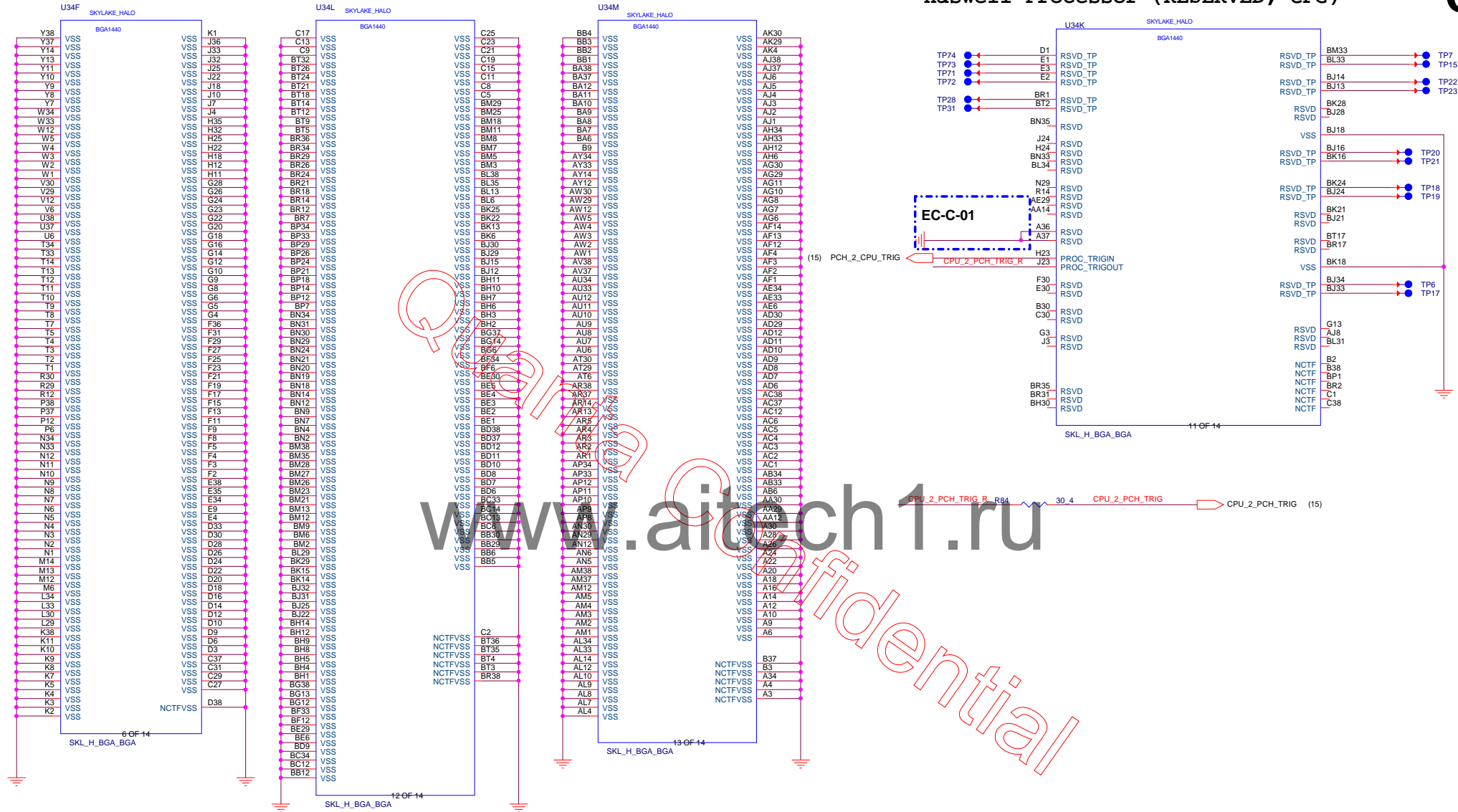


Unconnected for Processors without OPC.



Haswell Processor (GND)

Haswell Processor (RESERVED, CFG)

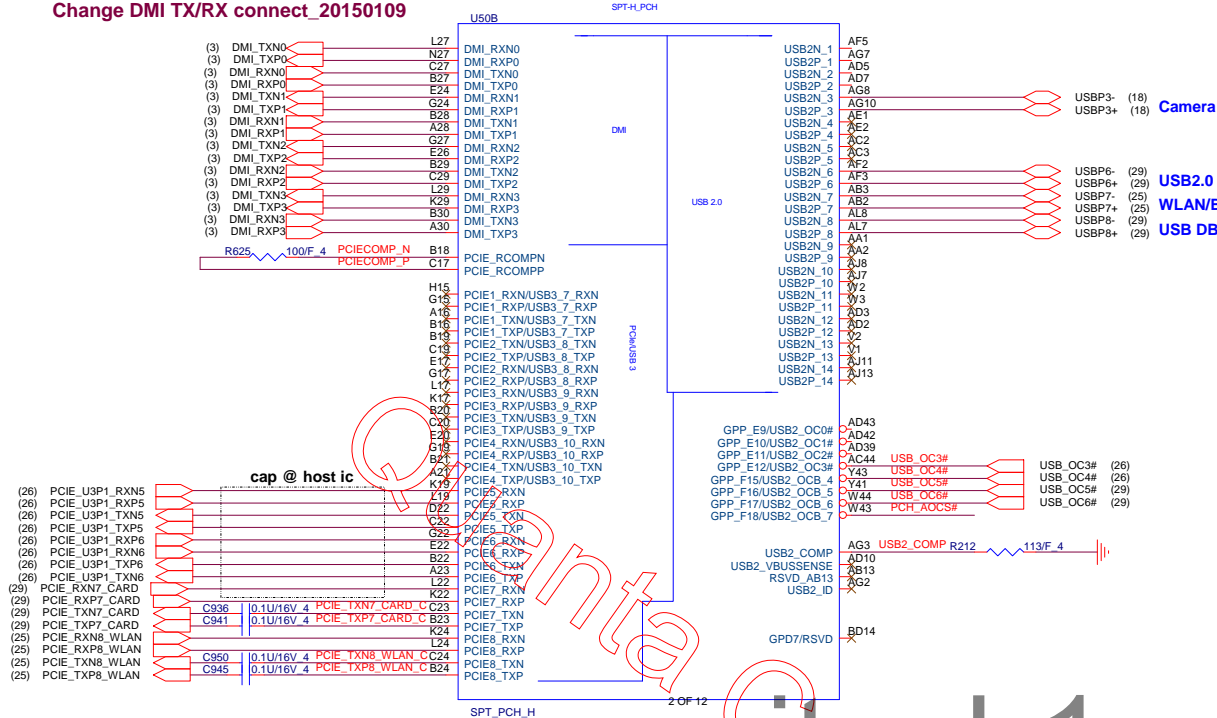


Change DMI TX/RX connect_20150109

USB3.1 Host x2

Cardreader(DB)

WLAN



GPU Strap

DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF
SAMPLED LOW
ELSE
DIFFERENTIAL

DGPU_PWROK_Q *10K 4 R723

RING OSCILLATOR BYPASS

DGPU_HOLD_RST# 100K 4 R726

XTAL INPUT FREQUENCY[0]

GPU_EVENT# *100K 4 R725

XTAL INPUT FREQUENCY[1]

GF_XON *10K 4 R344

DGPU_EVENT#-- For BIOS check

GPU_OVERT#_PCH *10K 4 R701

GPU_EVENT# 10K 4 R714

DGPU_HOLD_RST# *10K 4 R716

GF_XON 10K 4 R352

DGPU_PWROK_Q 10K 4 R719

GC6FBN_Q 10K 4 R427

SIO_EXT_SMI# 10K 4 R702

EC_RCIN# 10K 4 R248

EC-B-19

EC-B-10

PU at USB3.1 host

USB_OC5# 10K 4 R703

USB_OC3# 10K 4 R724

USB_OC4# 10K 4 R713

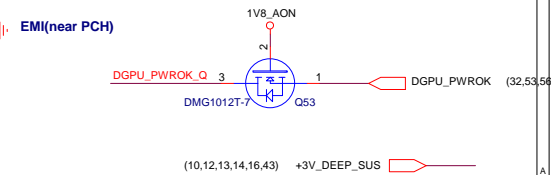
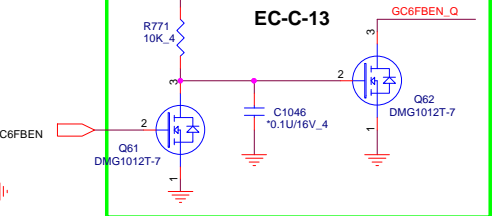
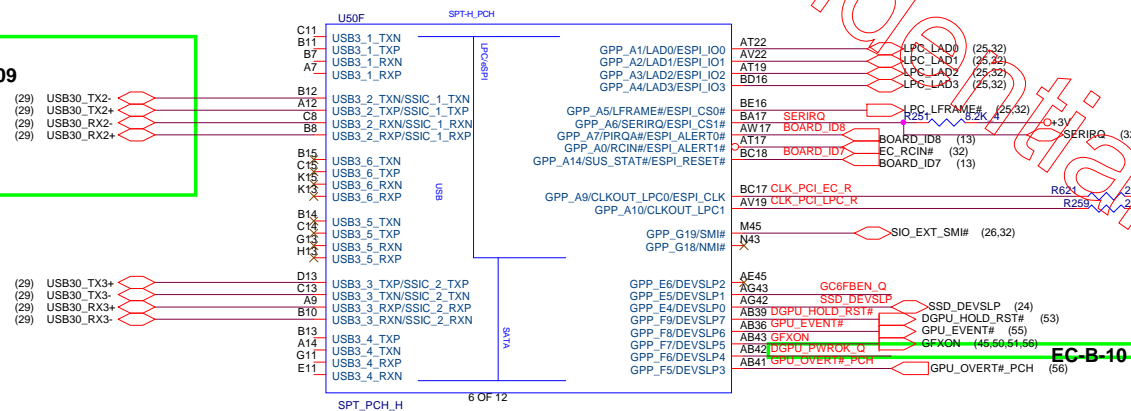
USB_OC6# 10K 4 R705

PCH_AOC5# 10K 4 R704

EC-B-09

USB3.0 (DB)

USB3.0 (DB)

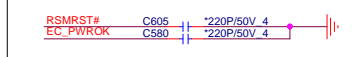
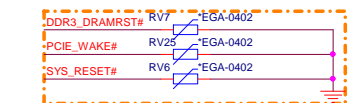
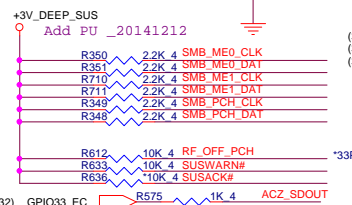


HDA Bus(CLG)

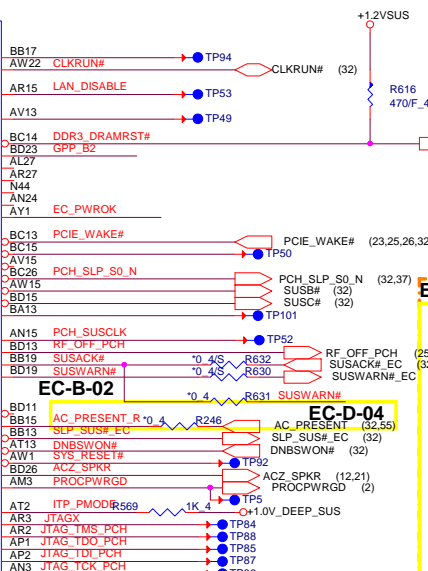
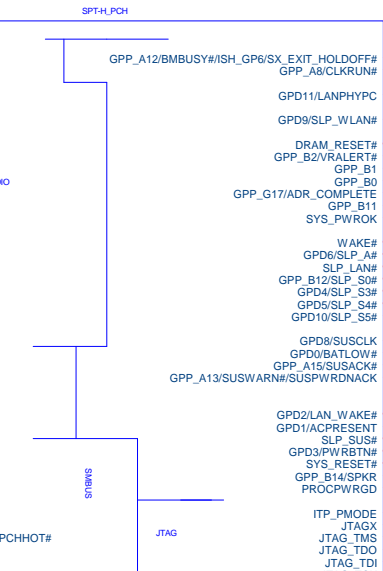
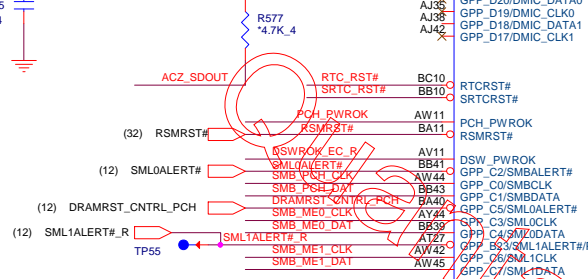


Reserve for EMI

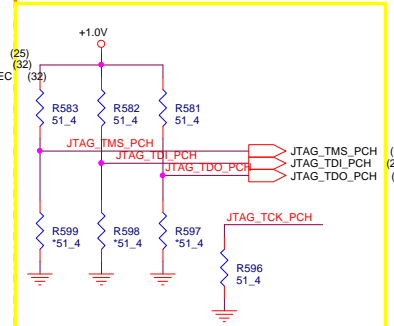
Change R2032 from 33 to 30_20141218



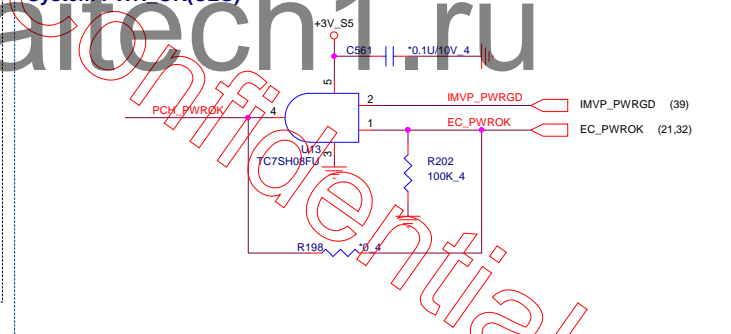
EMI



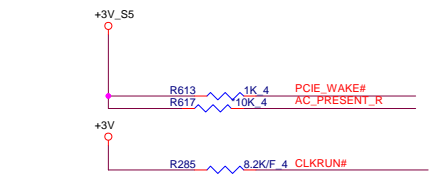
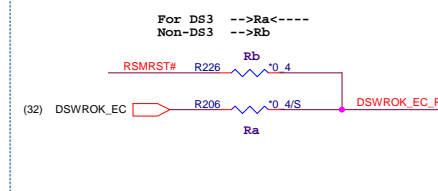
EC-D-07



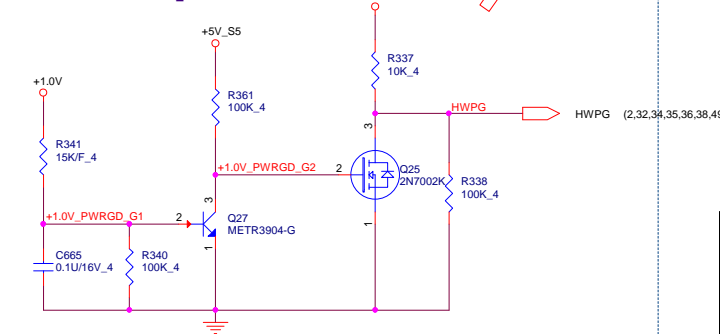
System PWR OK(CLG)



For DS3 Sequence

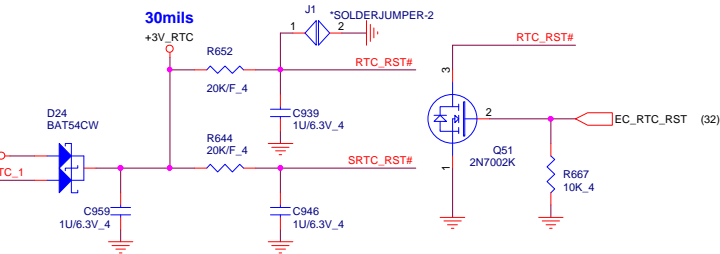
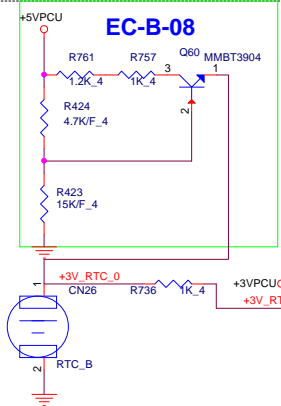


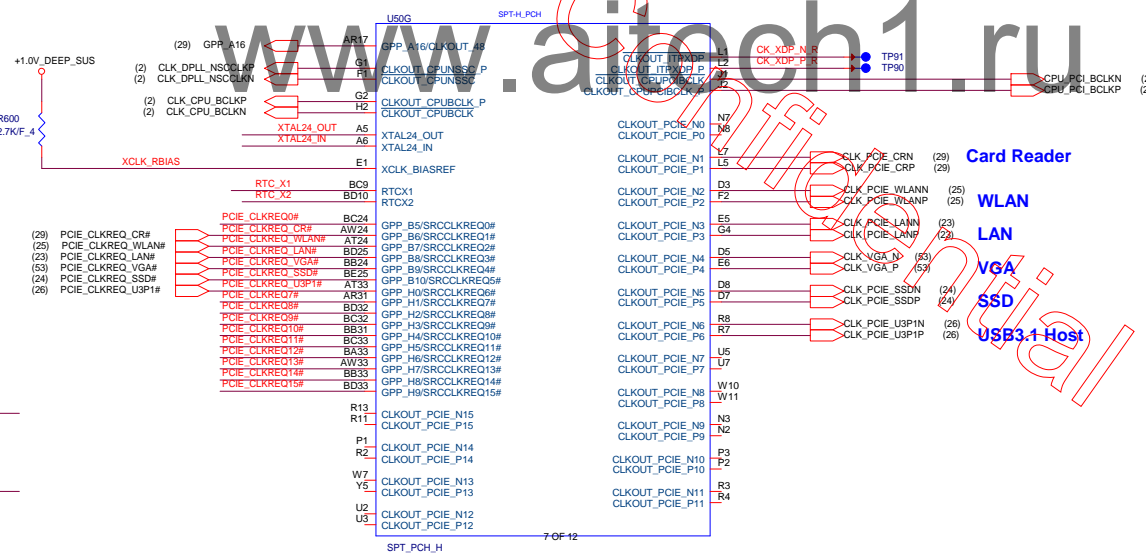
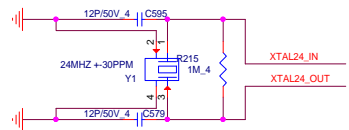
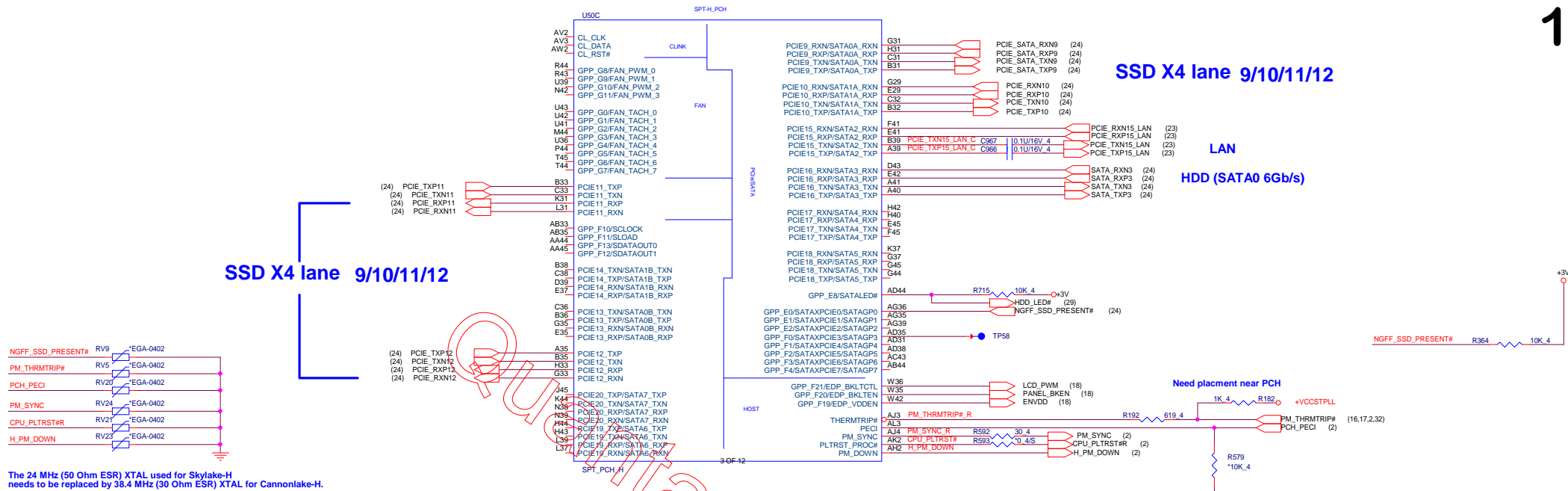
For HWPG Sequence



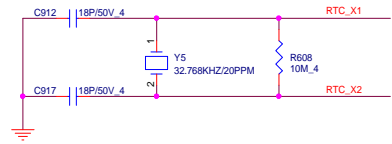
RTC Circuitry(RTC)

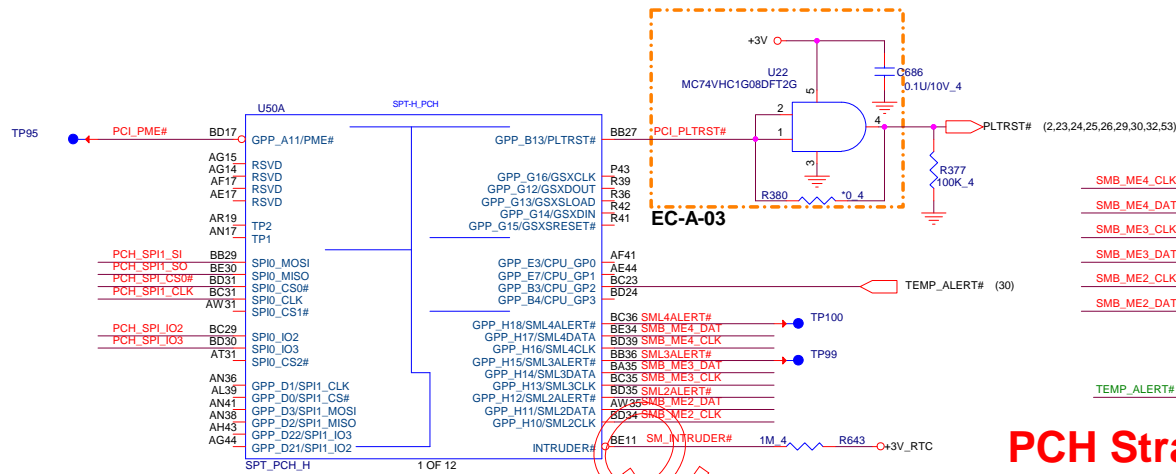
RTC Power trace width 20mils.





RTC Clock 32.768KHz

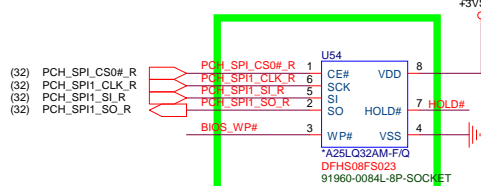




PCH SPI ROM (CLG)

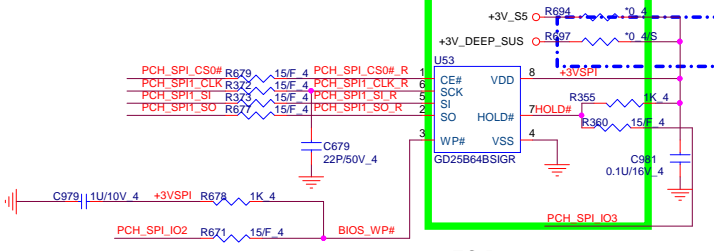
Vendor	Size	P/N
EON		
Winbond	16MB	AKE3DZN0N01
GigaDevice		
Socket		DFHS08FS023

4M SPI ROM Socket



U2003&U2004 footprint must overlap

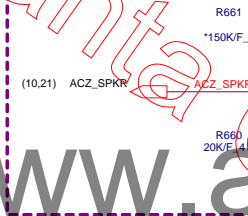
PCH SPI ROM (CLG)



EC-B-16

TOP SWAP OVERRIDE STRAP

HIGH: TOP SWAP
ENABLED (CRB)
DISABLED (DEFAULT)



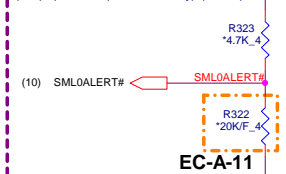
NO REBOOT IF SAMPLED HIGH

HIGH: Enable No Reboot mode.
This function is useful when running
TP/XP/DC.
LOW: Disable "No Reboot"
mode. (Default)



TLS CONFIDENTIALITY ENABLED

HIGH: T Enable Intel ME Crypto Transport
Layer Security
(TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport
Layer Security
(TLS) cipher suite (no confidentiality). (Default)

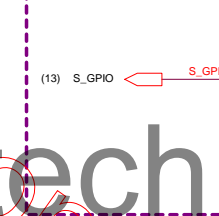


EC-A-11

PCH Strap Pin

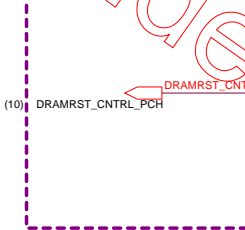
BOOT SELECT STRAP

HIGH: LPC
LOW: SPI
(Default)



ESP/LPC SELECT STRAP

HIGH: eSPI is selected for EC
LOW: LPC is selected for EC
(Default)



RESERVED

This strap should
sample HIGH.
There should NOT be any
on-board device
driving it to opposite
direction during
strap sampling.



RESERVED

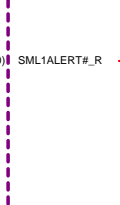
This strap should
sample HIGH.

There should NOT be any
on-board device
driving it to opposite
direction during
strap sampling.



RESERVED

This strap should
sample LOW.
There should NOT be any
on-board device
driving it to opposite
direction during
strap sampling.



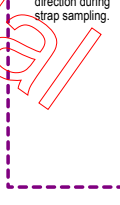
RESERVED

This strap should
sample HIGH.
There should NOT be any
on-board device
driving it to opposite
direction during
strap sampling.



RESERVED

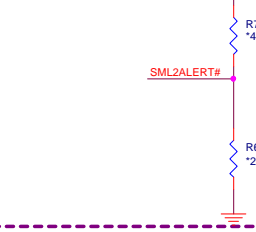
This strap should
sample HIGH.
There should NOT be any
on-board device
driving it to opposite
direction during
strap sampling.



ESPI FLASH SHARING MODE

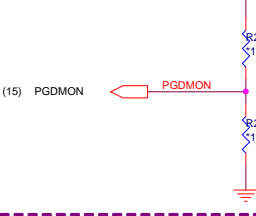
HIGH: SLAVE ATTACHED
FLASH SHARING
LOW: 0: MASTER ATTACHED
FLASH SHARING

This strap should
sample LOW.
driving it to opposite
direction during
strap sampling.
There should NOT be any
on-board device



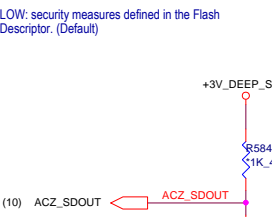
DFX TEST MODE QUALIFIER FOR OTHER

OPEN SAMPLED
LOW



TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This
strap should only be asserted high using external
pull-up in manufacturing/debug environments ONLY. (CRB)
LOW: security measures defined in the Flash
Descriptor. (Default)



Quanta Computer Inc.

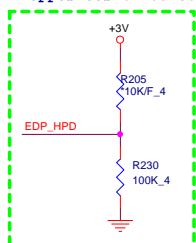
PROJECT :

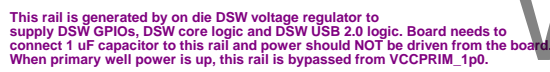
PCH 4/6 (GPIO/MISC)

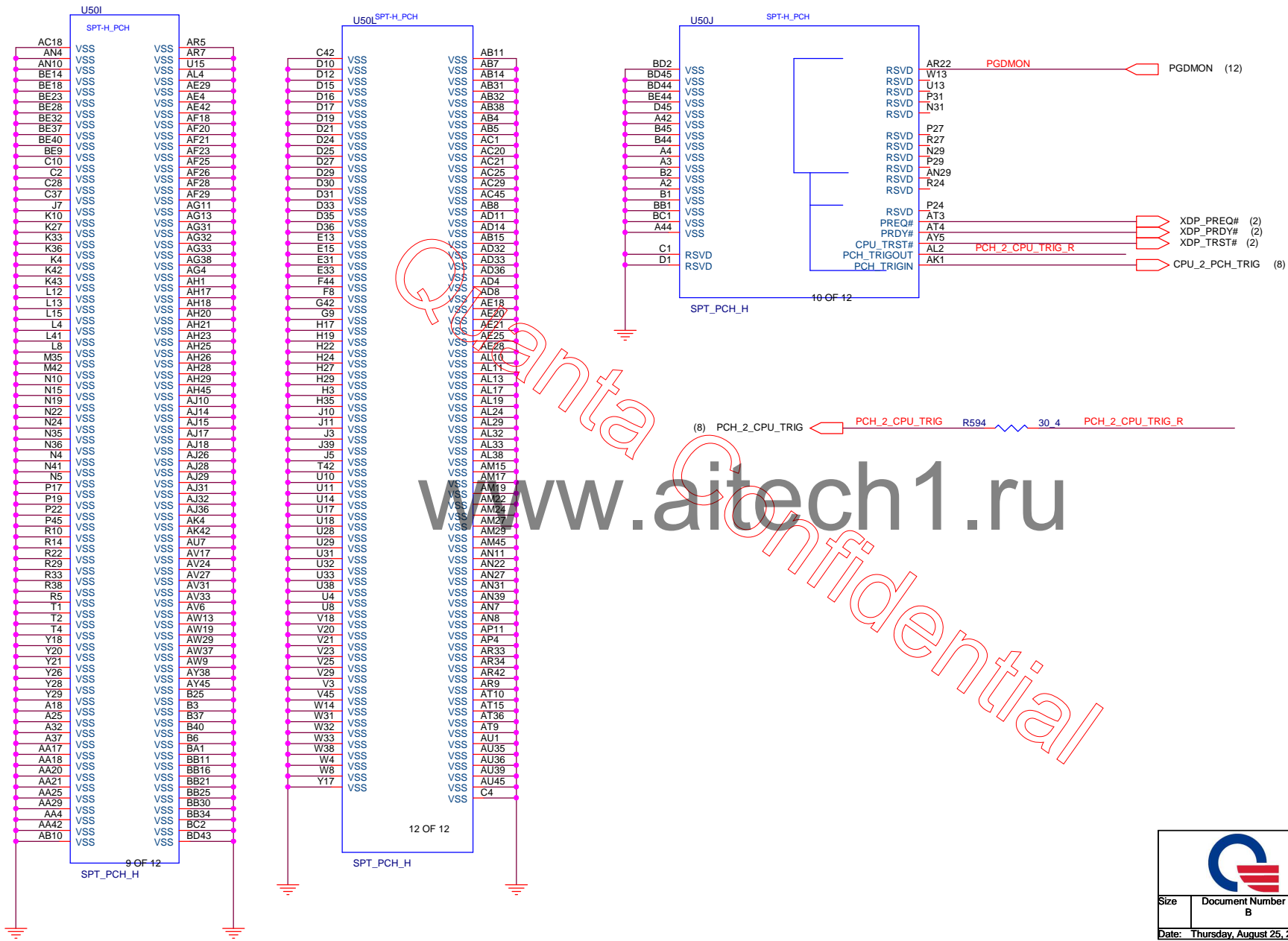
Size	Document Number	Custom	Rev
			2A
Date:	Thursday, August 25, 2016	Sheet	12 of 68

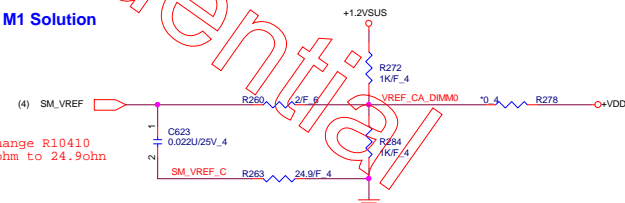
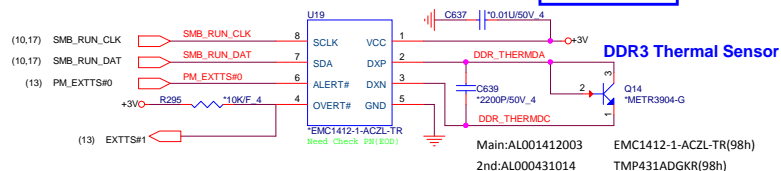
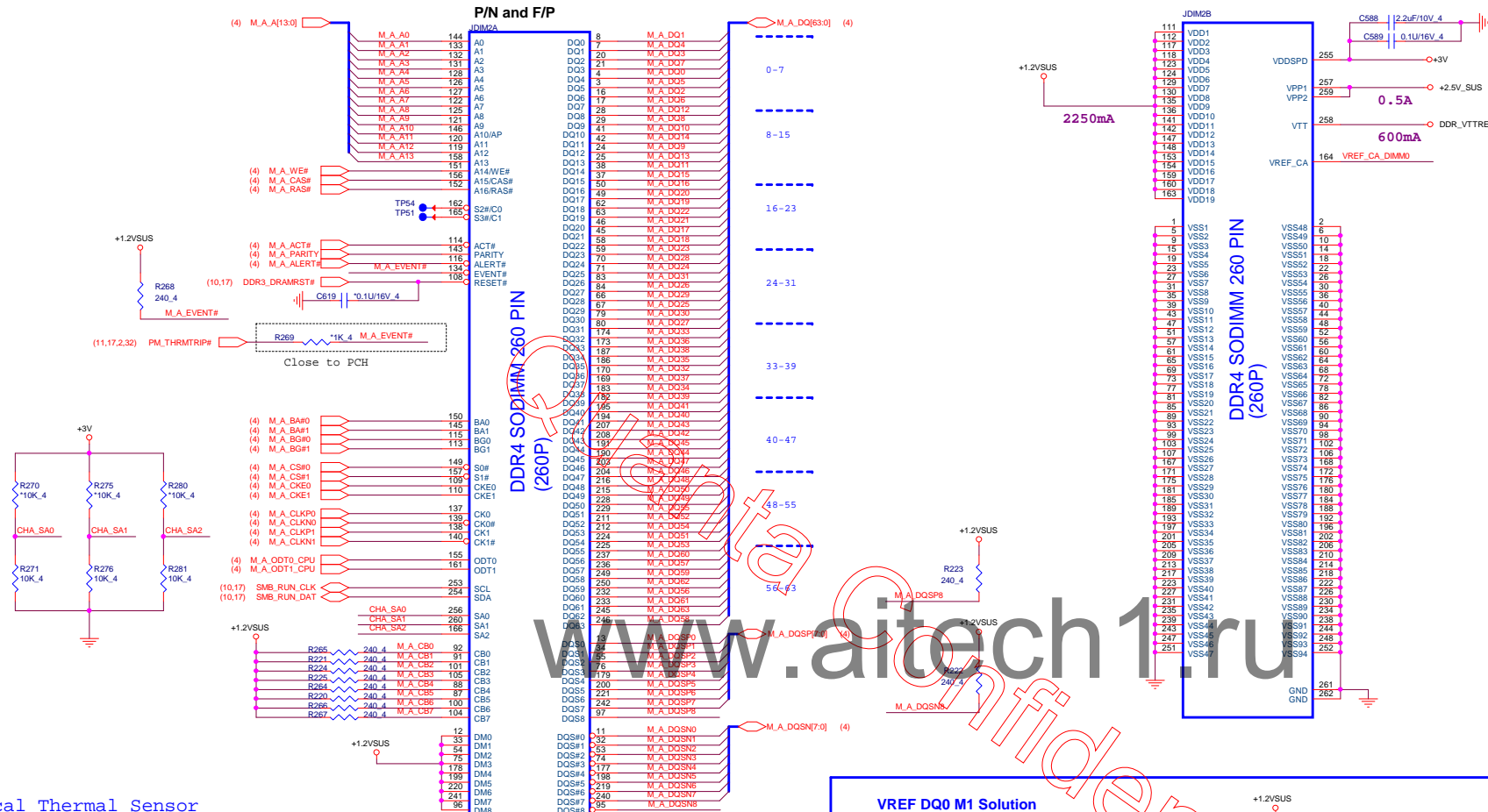


NL8C cable pin6 gnd =low,
NL9 cable pin6 NC and NL9 have ext PU (R629)=high
BoardID0&1 should be ext PU

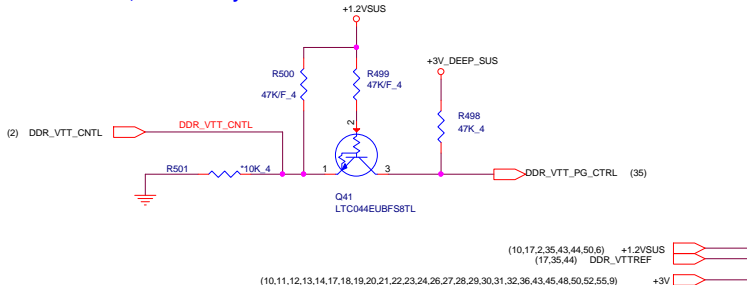






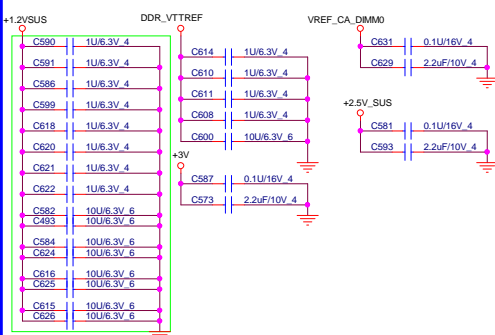


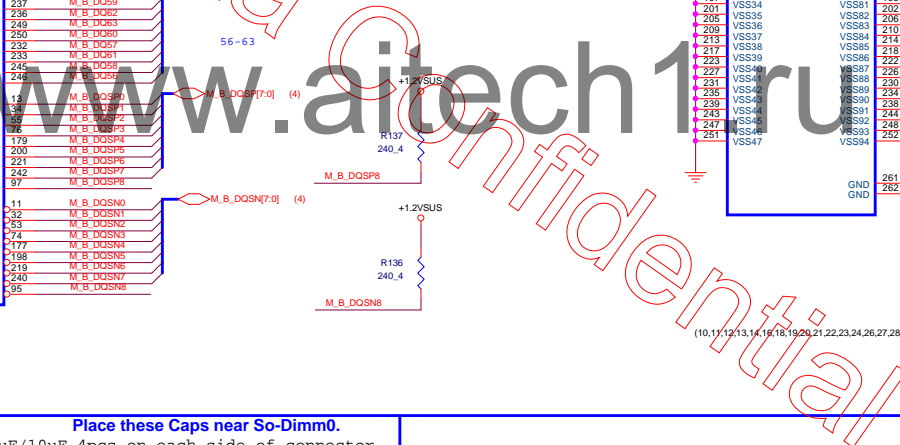
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU



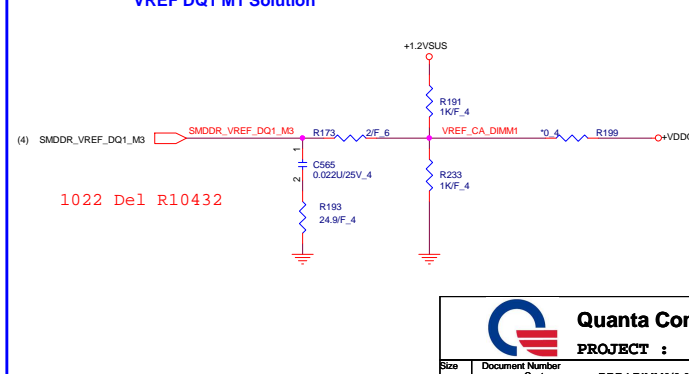
Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

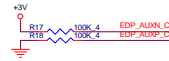
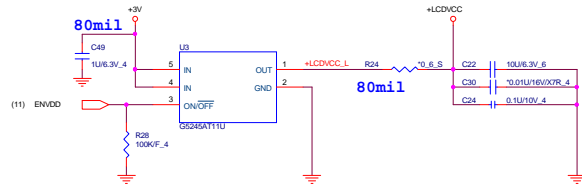




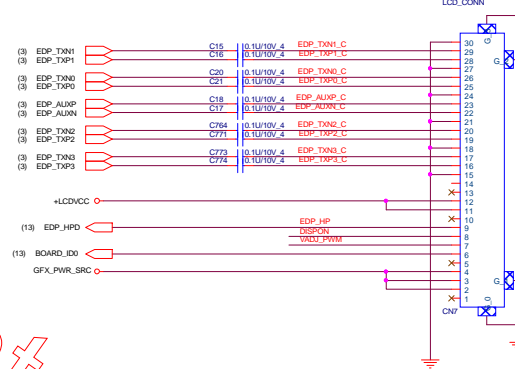
VREF DQ1 M1 Solution



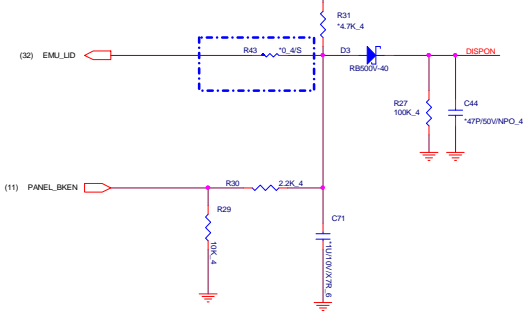
LCDVCC



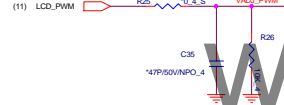
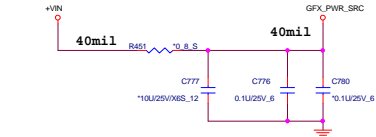
30Pin eDP CN



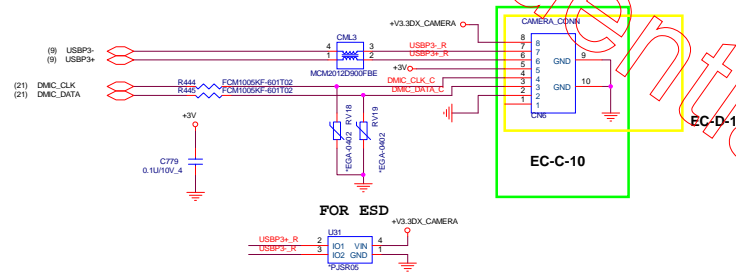
Back light



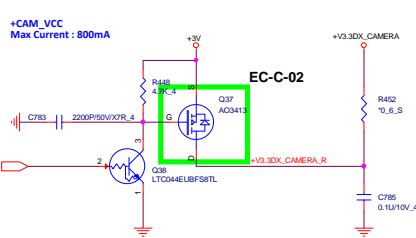
GFX_PWR_SRC

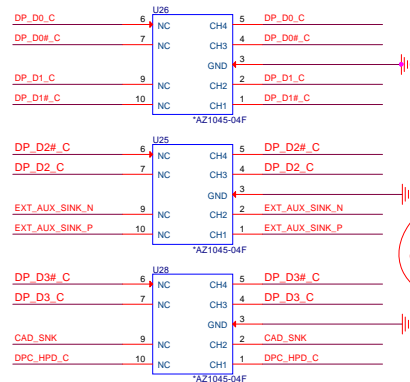


CAMERA/DMIC CONN

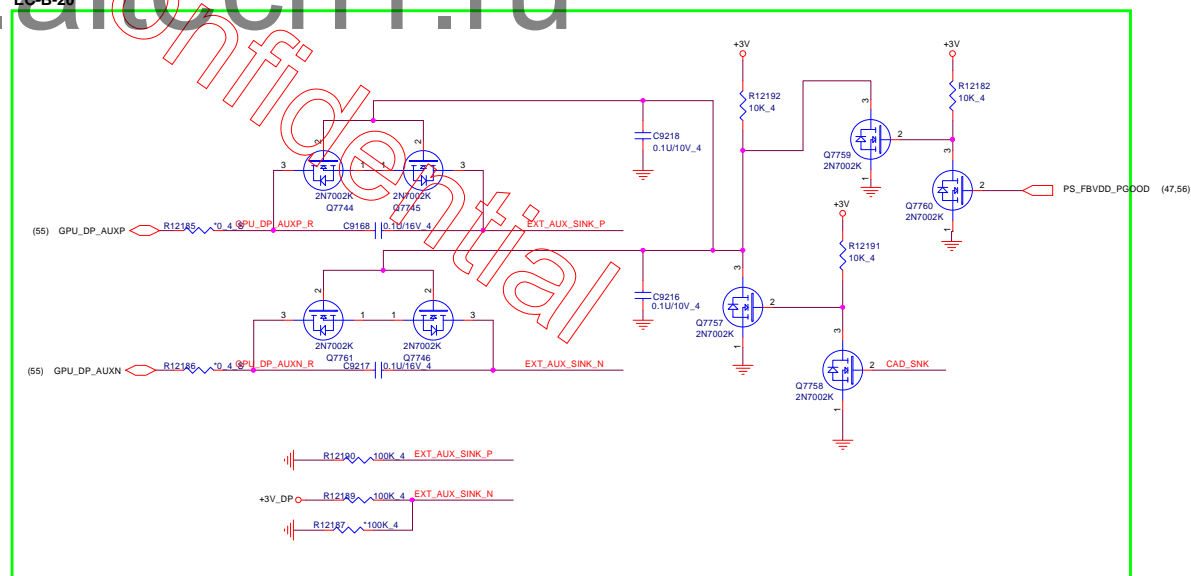
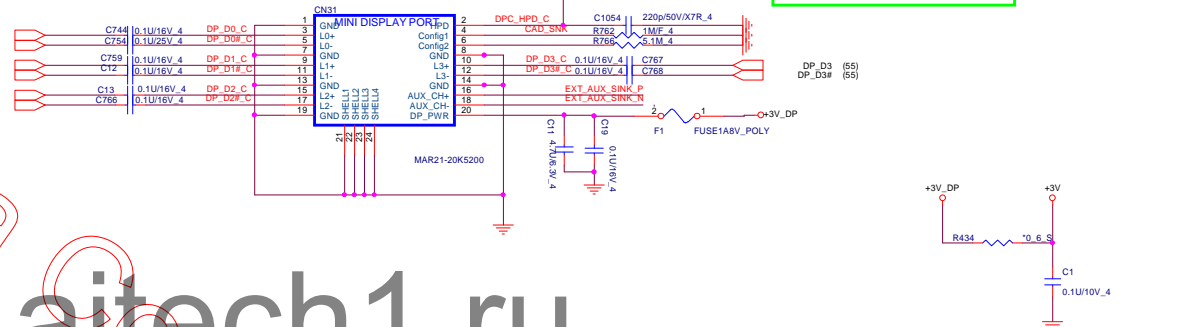
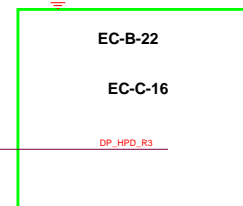
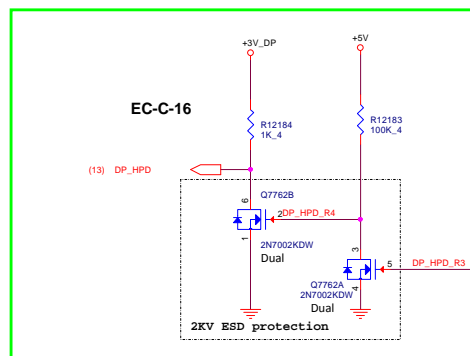


CAMERA VCC Control



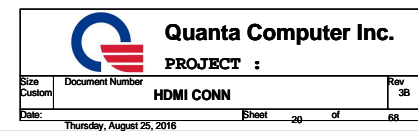


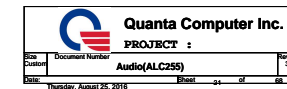
Layout note:Place close to HDMI Conn



(10,11,12,13,14,16,17,18,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,48,50,52,55,9) +3V

(20,21,22,24,30,31,43,45,52,63) +5V





Reserve for Input attenuation
To have optimization output power

Placement C4609
and then C4611

Close to IC

need to Close to connector
Reserve for EMI Depression

need to very
Close to IC

Output Gain Table

R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

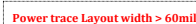
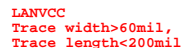


Quanta Computer Inc.

PROJECT :

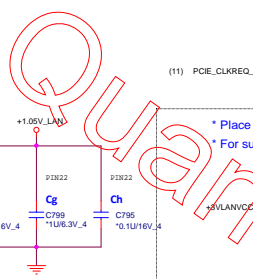
Size Custom Document Number Amplifer(ALC1003) Rev 3B

Date: Thursday, August 25, 2016 Sheet 22 of 68

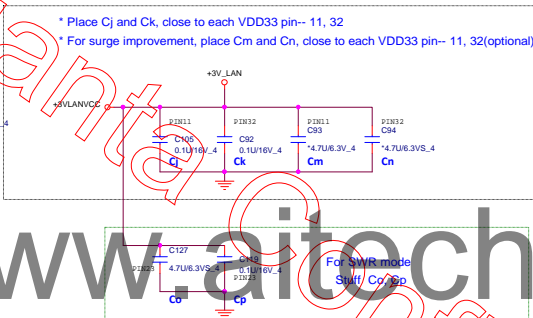


Trace < 30 mil
Width > 60 mil

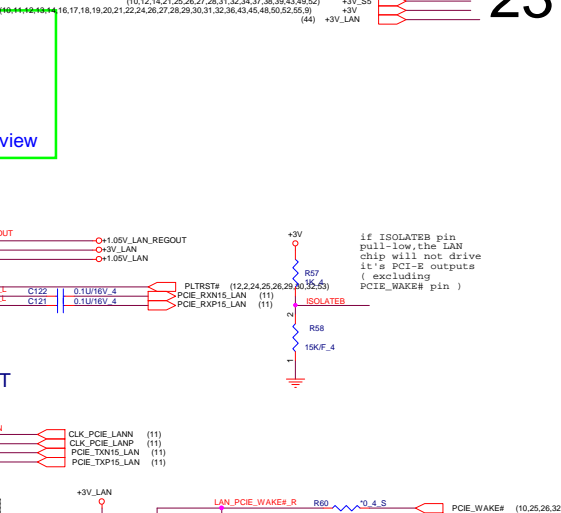
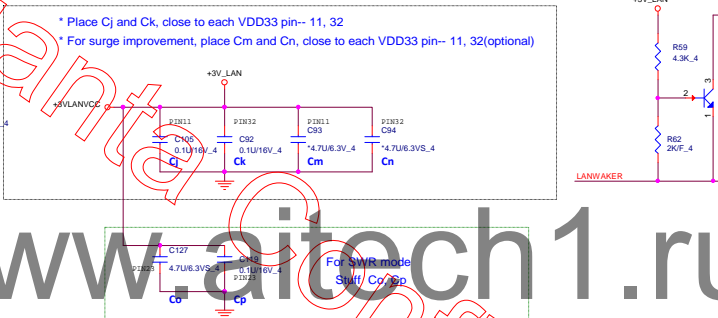
For SWR mode
 Stuff La, Ca ,Cb
 NA : Ra, Ci



- * Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 22, 8 , 30
- * Place Cg,Ch
close to each VDD10 pin-- 22(reserved)



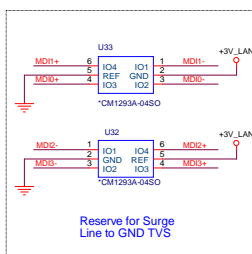
Remove For Not Using SWR mode



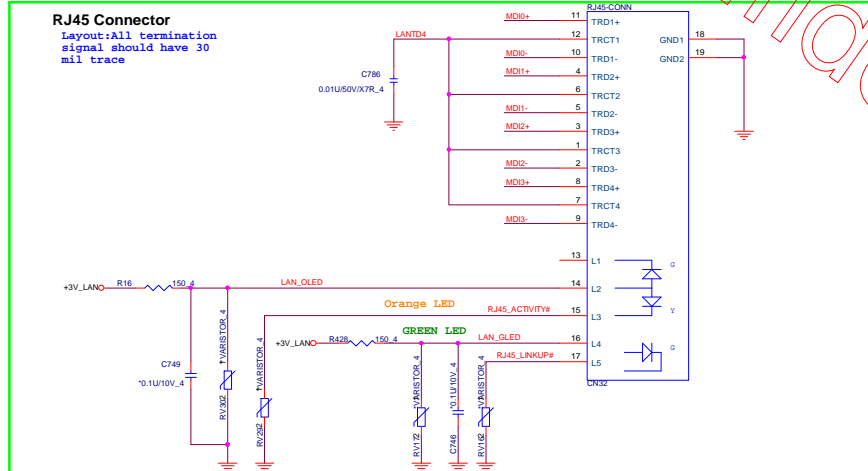
```
if ISOLATED pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```

www.aitech1.ru

EC-B-13



Reserve for Surge
Line to GND TVS



RJ45 Connector

Layout: All termination
signal should have 30
mil trace

SSD

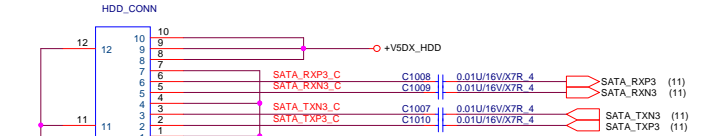
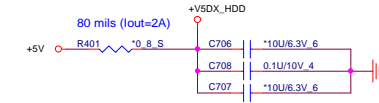
(10,11,12,13,14,16,17,18,19,20,21,22,23,26,27,28,29,30,31,32,36,43,45,48,50,52,55,9) +3V

(19,20,21,22,30,31,43,45,52,63) +5V

24

HDD

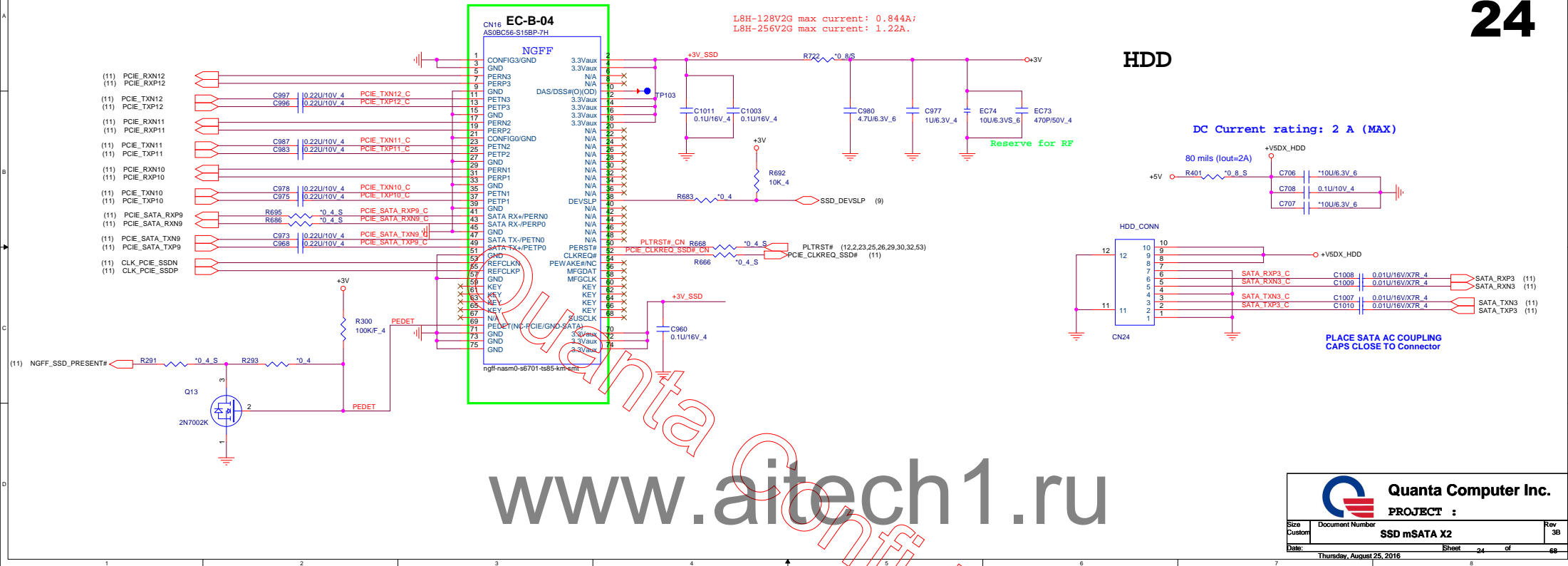
DC Current rating: 2 A (MAX)



PLACE SATA AC COUPLING CAPS CLOSE TO Connector

www.aitech1.ru

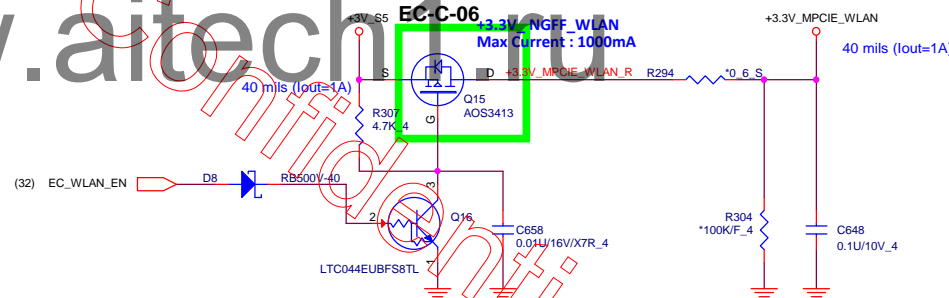
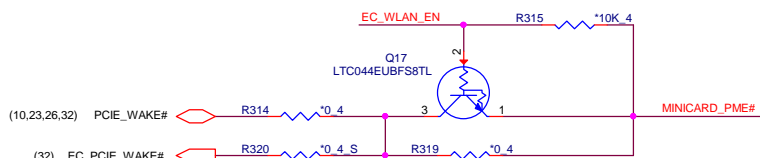
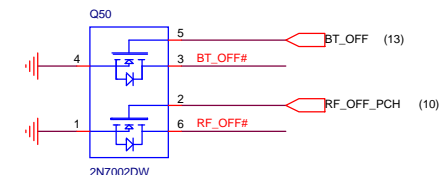
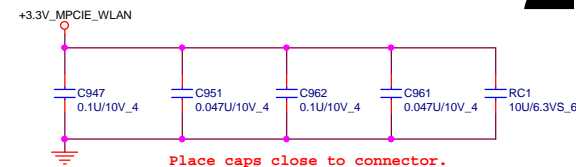
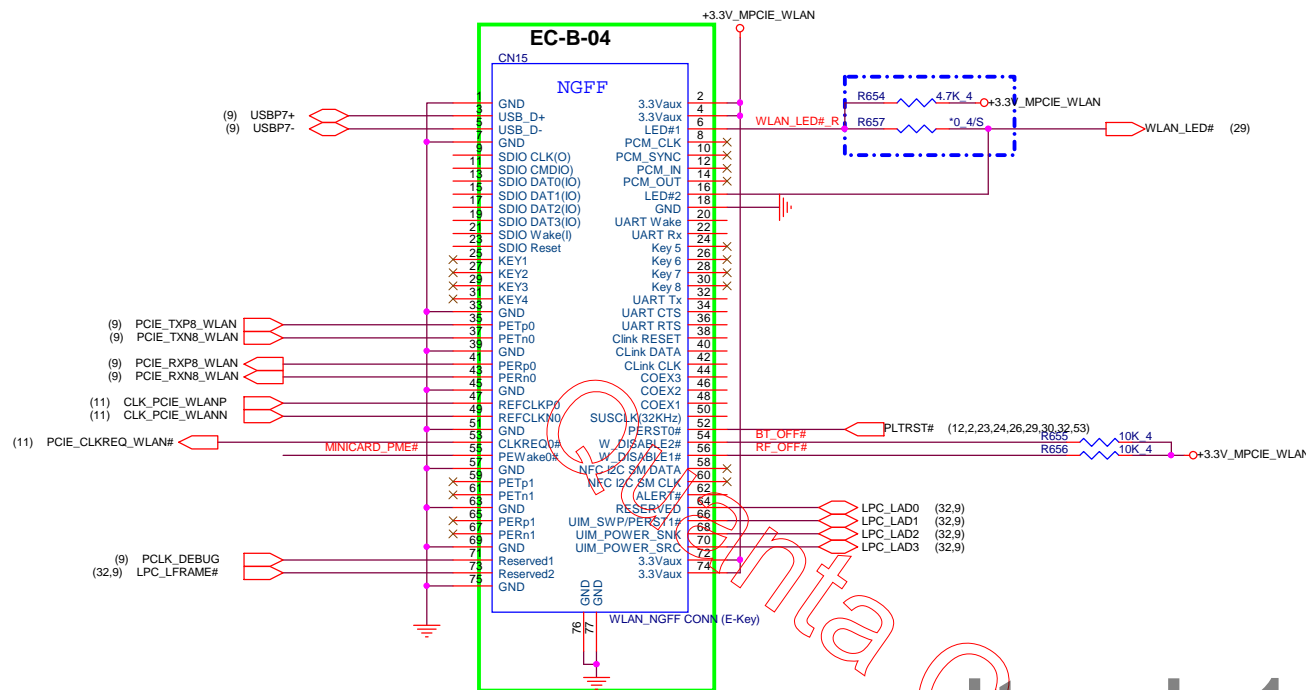
Quanta Computer Inc.			
PROJECT :			
Size Custom	Document Number	SSD mSATA X2	
Date:	Thursday, August 25, 2016	Sheet 24 of 68	Rev 3B

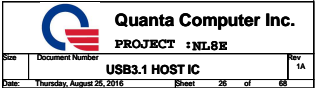


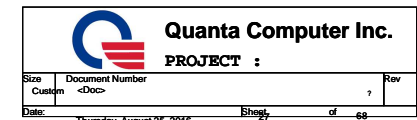
Mini PCIE Wifi/BT connector

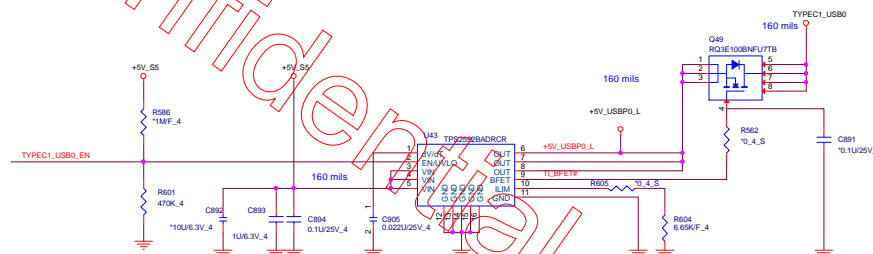
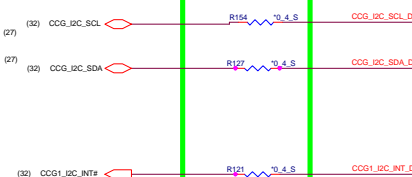
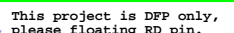
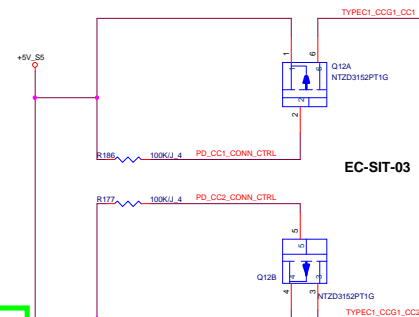
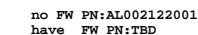
(10,12,14,21,23,26,27,28,31,32,34,37,38,39,43,49,52) +3V_S5
(21,38,44) +1.5V

25



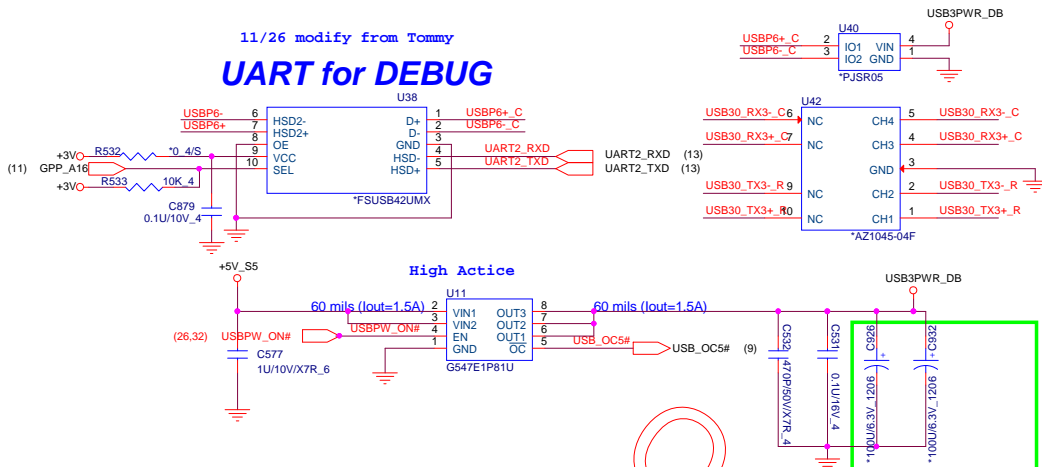




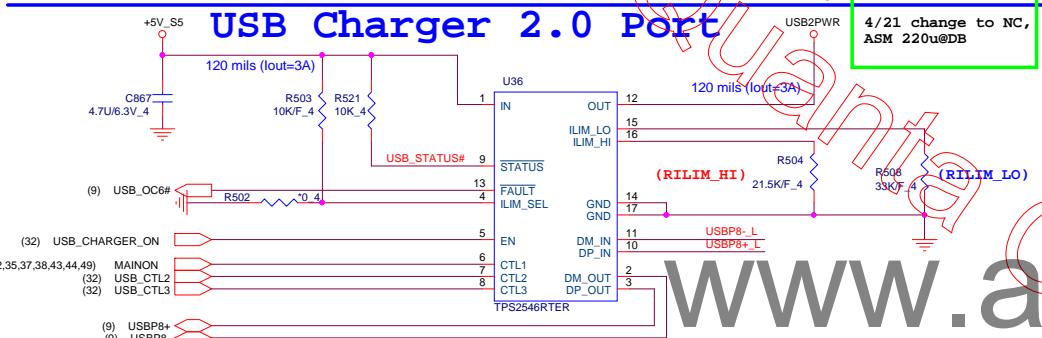


```
Rlim= (Ilim-0.7)/(3*0.00001)
      fix 0.9A
```


11/26 modify from Tommy UART for DEBUG



USB Charger 2.0 Port



RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used

If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.

The following equation programs the typical current limit:

$$I_{OS_typ}(mA) = \frac{50,500}{(R_{ILIM_XX}(k\Omega) + 0.1)}$$

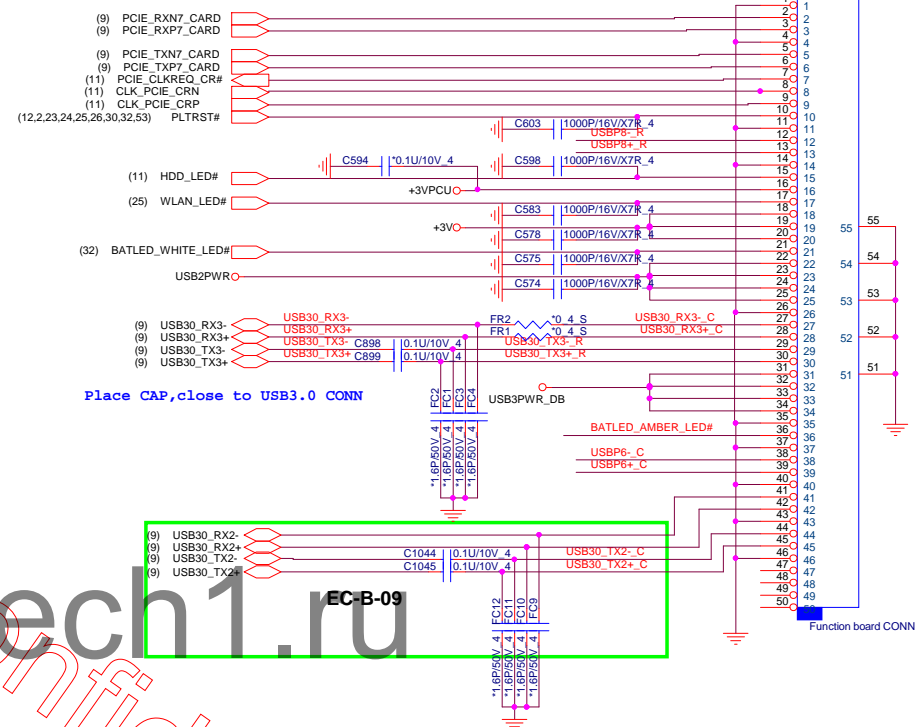
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

(10,26,28,34,35,36,37,39,40,41,42,43,44,45,46,47,49,50,51,52)
(10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,36,43,45,48,50,52,55,9)

+5V_S5
+3V

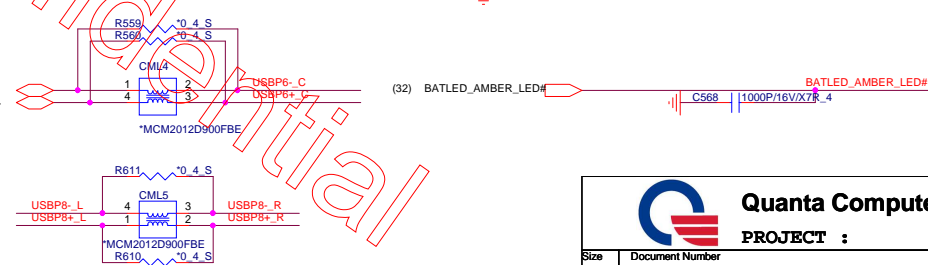
29

Board to Board



Place CAP, close to USB3.0 CONN

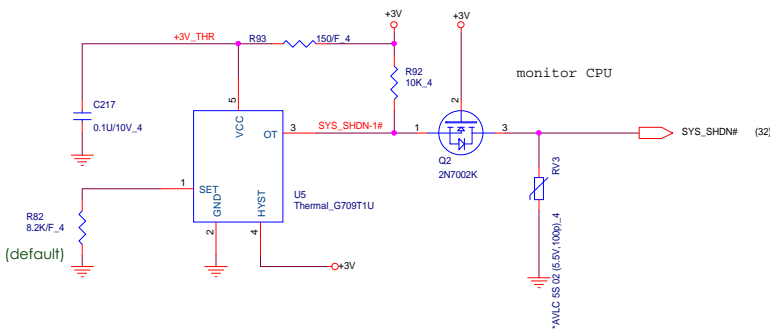
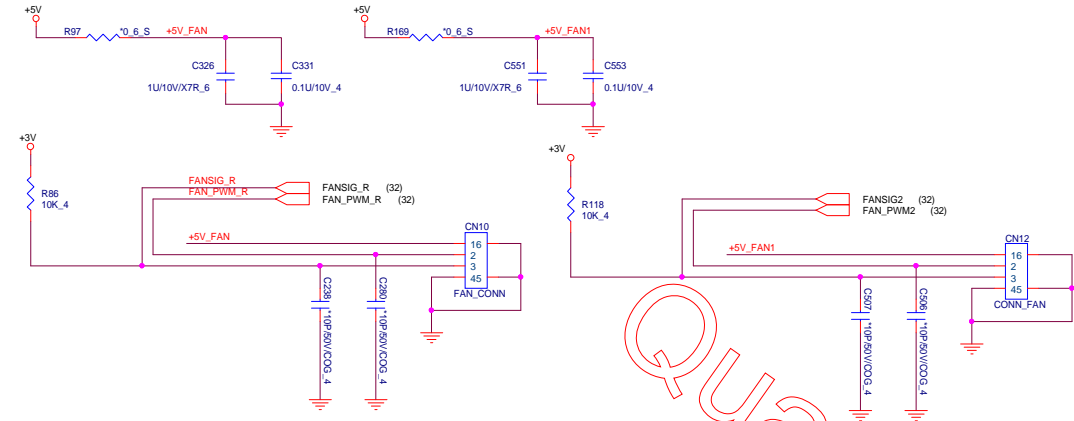
EC-B-09



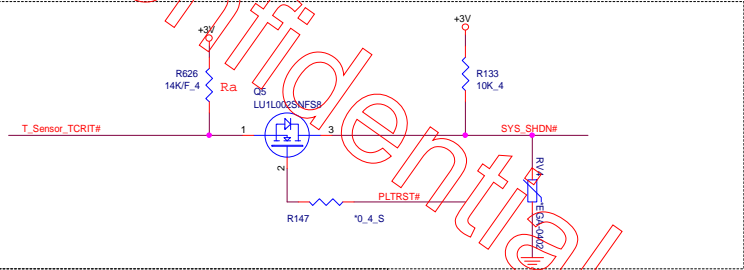
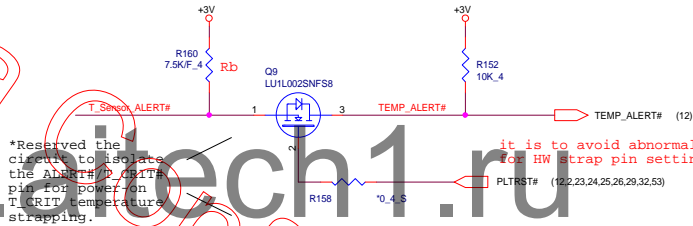
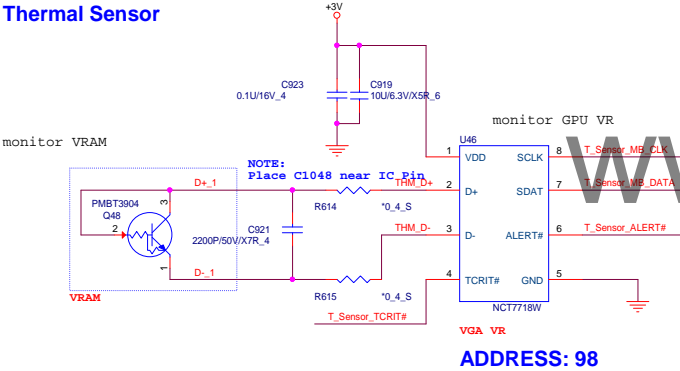
Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
Custom	USB2.0 X1/FUNCTION B	3B
Date:	Thursday, August 25, 2016	Sheet 29 of 68



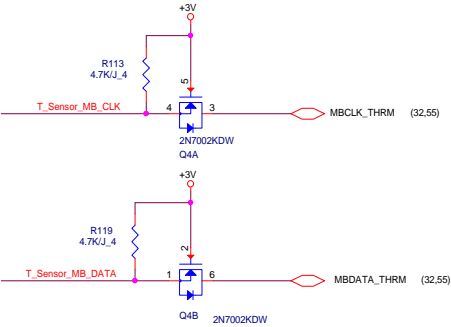
Thermal Sensor



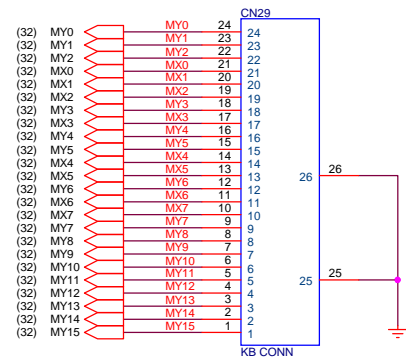
ALERT# /T_CRIT# Pull-up Resistor

	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
Rb	77°C	87°C	97°C	107°C	117°C
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

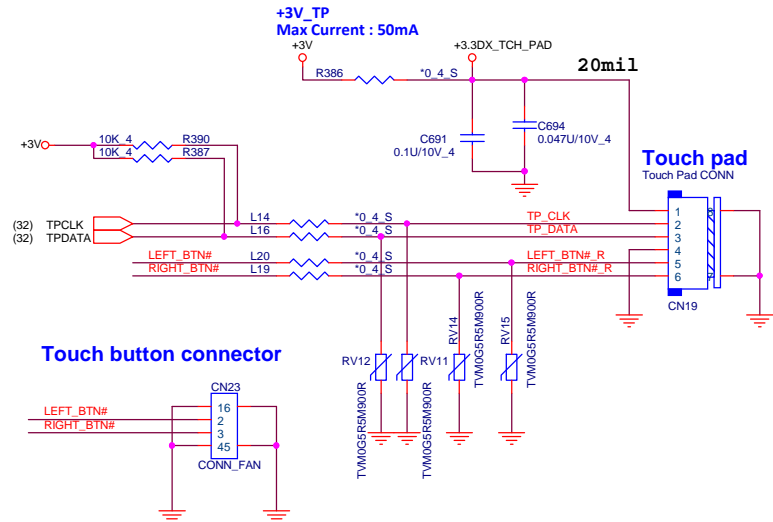
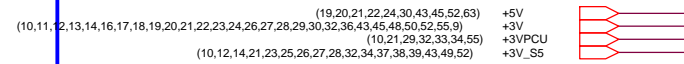


KEYBOARD

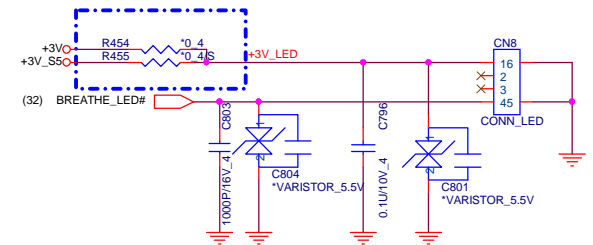
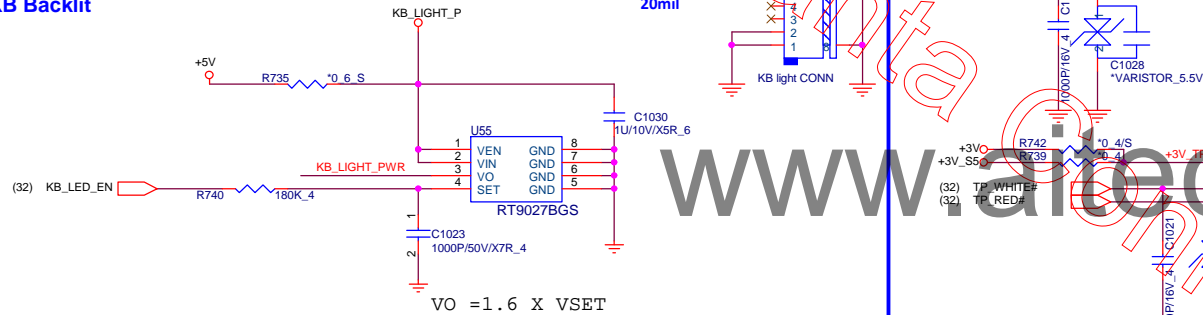


For EMI

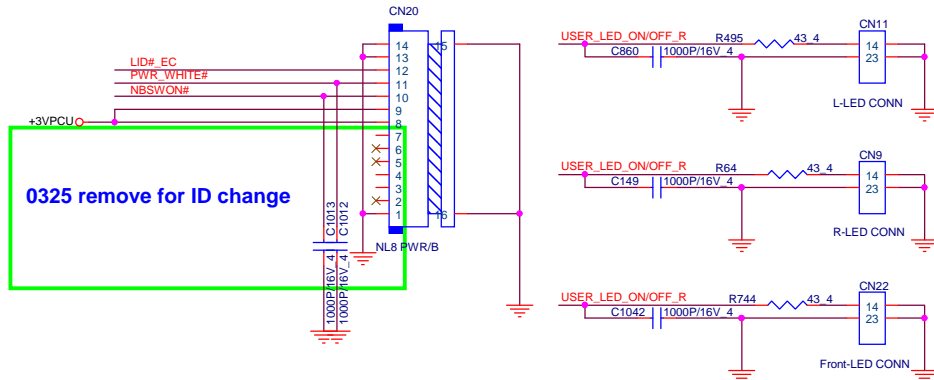
MY15 C731	220P/50V/X7R_4	C729	220P/50V/X7R_4	MY13
MY10 C726	220P/50V/X7R_4	C728	220P/50V/X7R_4	MY12
MY11 C727	220P/50V/X7R_4	C738	220P/50V/X7R_4	MY3
MY14 C730	220P/50V/X7R_4	C720	220P/50V/X7R_4	MY6
MX0 C735	220P/50V/X7R_4	C736	220P/50V/X7R_4	MX1
MY1 C733	220P/50V/X7R_4	C722	220P/50V/X7R_4	MX7
MY5 C717	220P/50V/X7R_4	C721	220P/50V/X7R_4	MX6
MX3 C739	220P/50V/X7R_4	C725	220P/50V/X7R_4	MY9
MX2 C737	220P/50V/X7R_4	C724	220P/50V/X7R_4	MY8
MY0 C732	220P/50V/X7R_4	C716	220P/50V/X7R_4	MY7
MX5 C719	220P/50V/X7R_4	C716	220P/50V/X7R_4	MY4
MX4 C718	220P/50V/X7R_4	C734	220P/50V/X7R_4	MY2



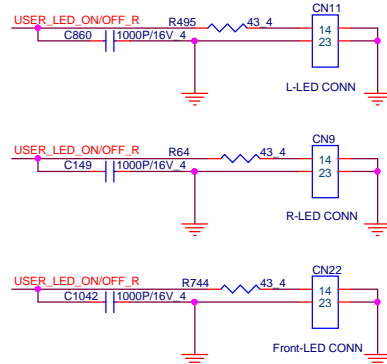
KB Backlit



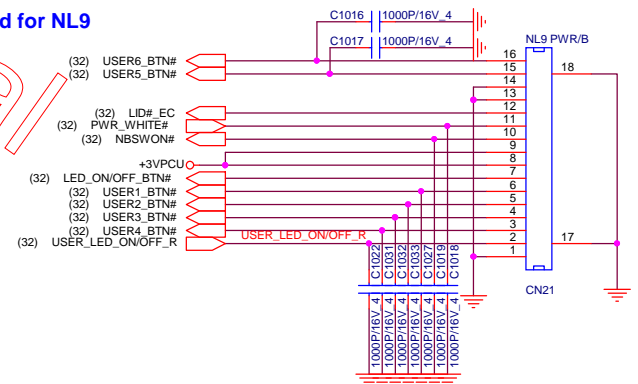
Power board for NL8



LED CONN



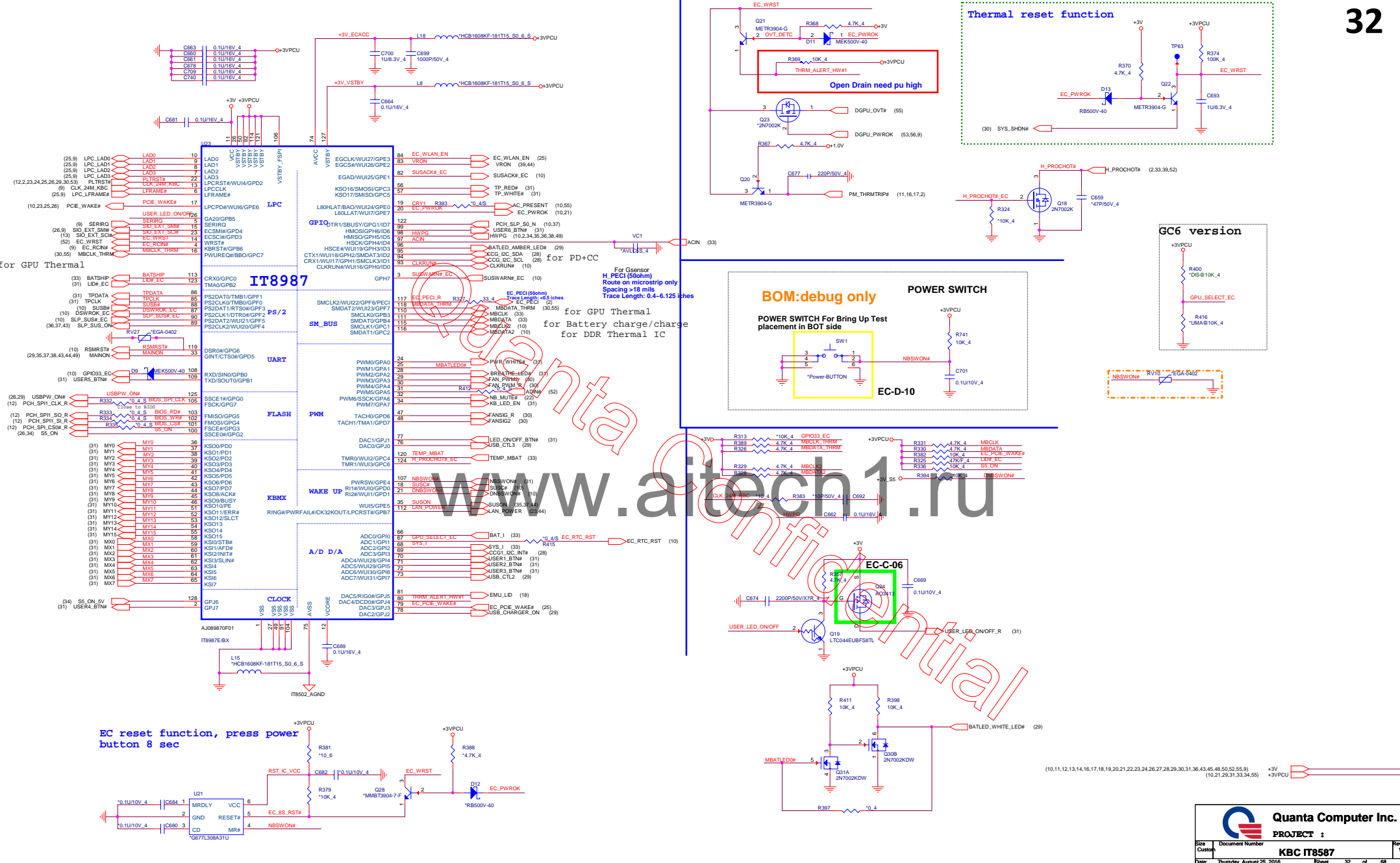
Power board for NL9



Quanta Computer Inc.

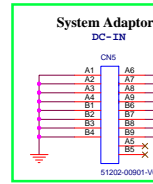
PROJECT :

Size	Document Number	Rev
Custom	KB/TP/LID	38
Date:	Thursday, August 25, 2016	Sheet 31 of 68



(18,34,35,36,39,40,41,42,47,50,52,63) +VA
(10,21,29,31,32,34,55) +VIN
+3VPCU

230W for N17E-G1 : N17P-G1
180W for N16E-GT (970M)
150W for N16P-GX (960M) : N16E-GS (965M)
120W for N16P-GT (950M)



Do Not add test pad on BATDIS_G signal

Place this ZVS close to Diode away +VIN

EMI request for ISN

5m ohm for 180W adapter

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to EC

For ISN

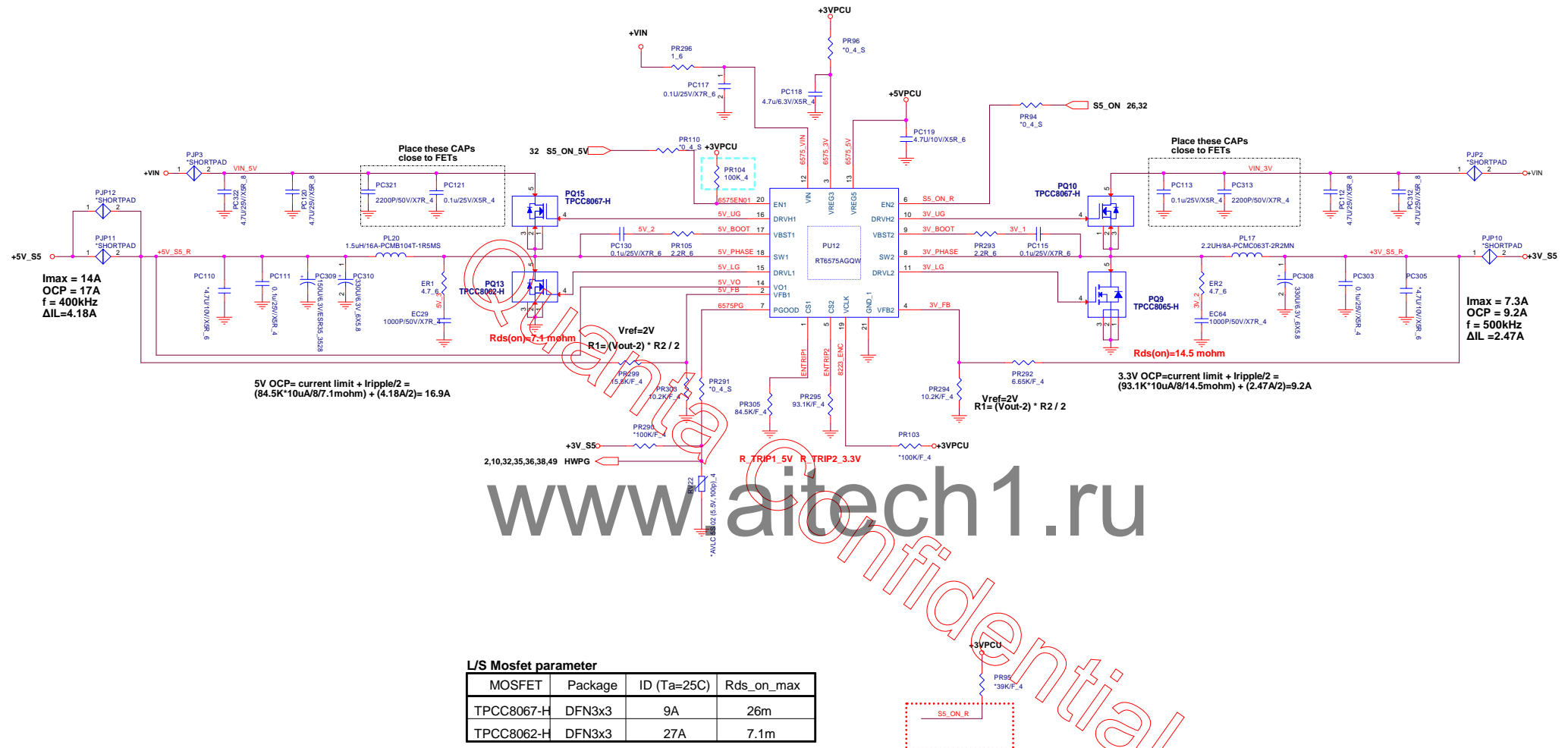
Place this cap close to EC

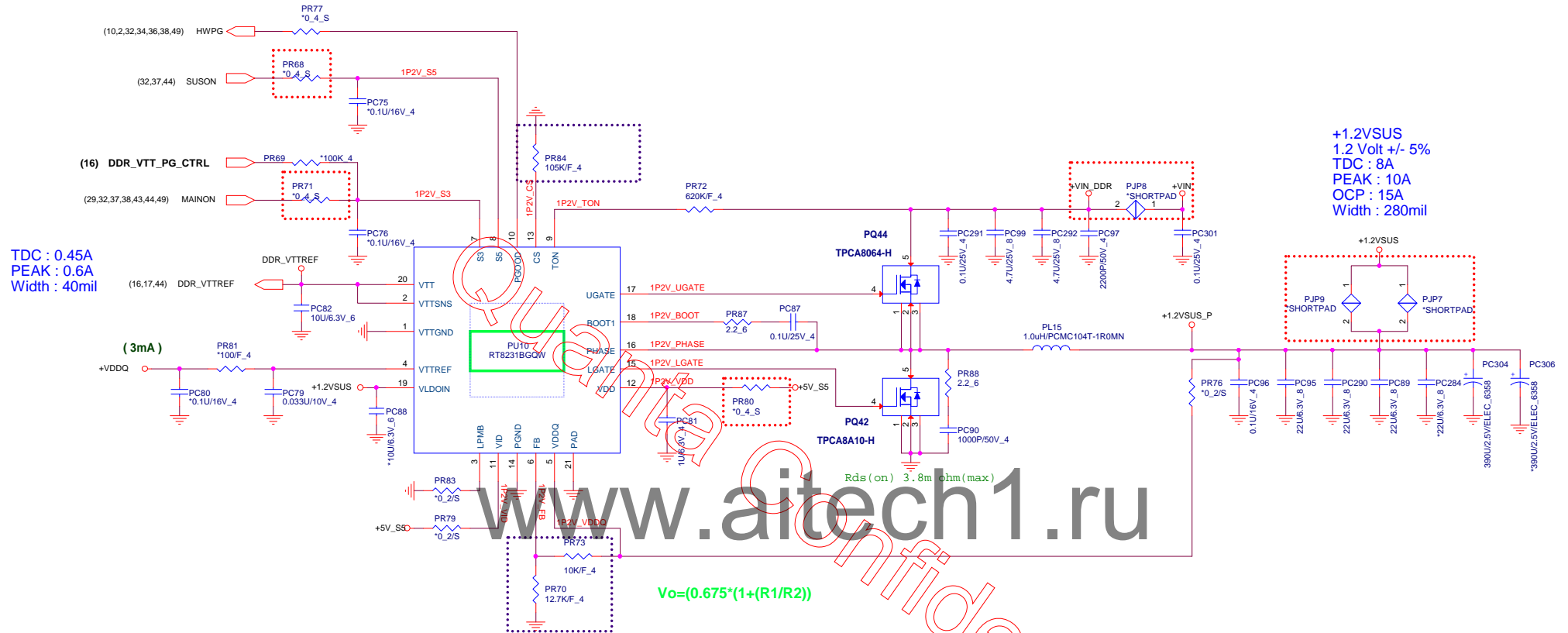
AC adapter	330W	230W	180W
Adapter ID-pin R (Ω, 1%)	4640Ω	1910Ω	1000Ω
EC delection V	2.626 ~ 3.056	2.149 ~ 2.590	1.663 ~ 2.109

PM決議不導入

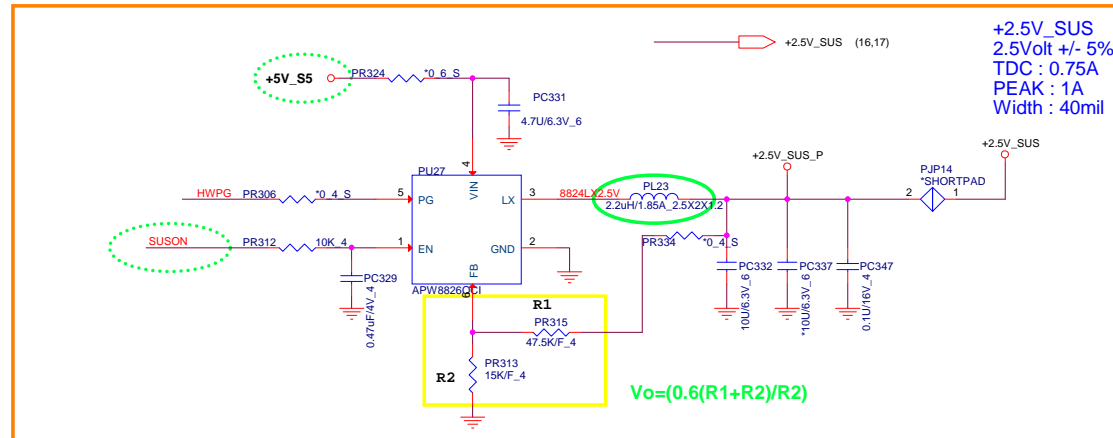
ACDET=17.2V

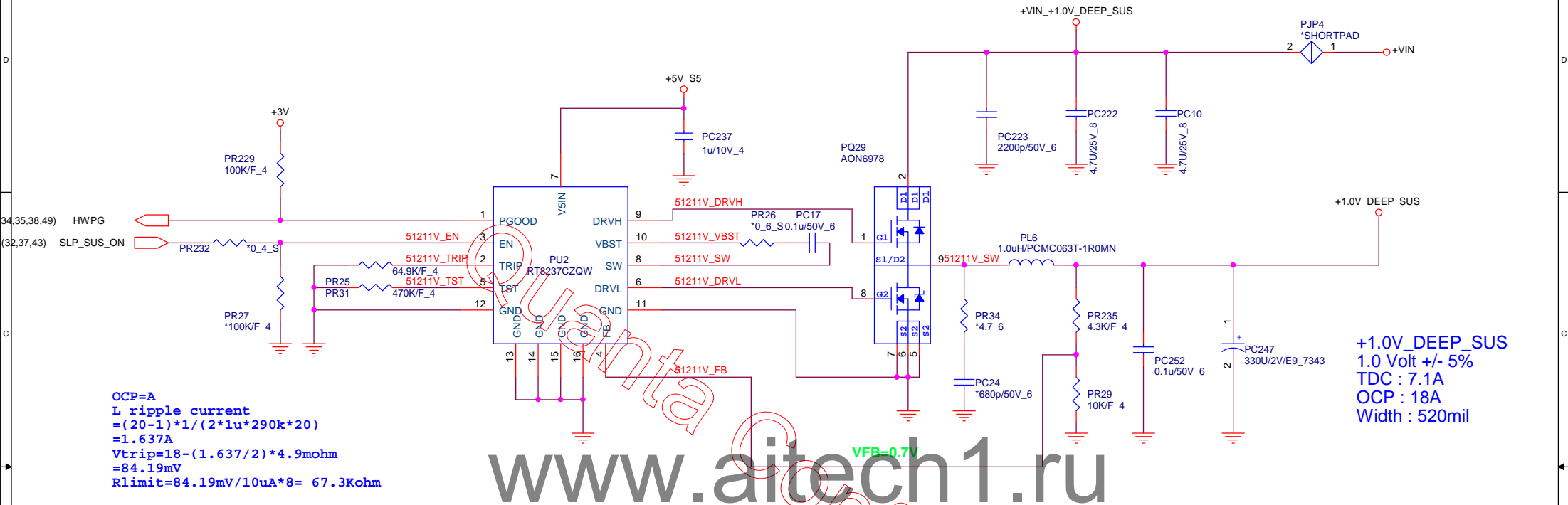
VIDCHG = 8 or 16 × (VSRN - VSRP)





7/09 Chaneg DDR3L to DDR4
Adding +2.5V Power Rail



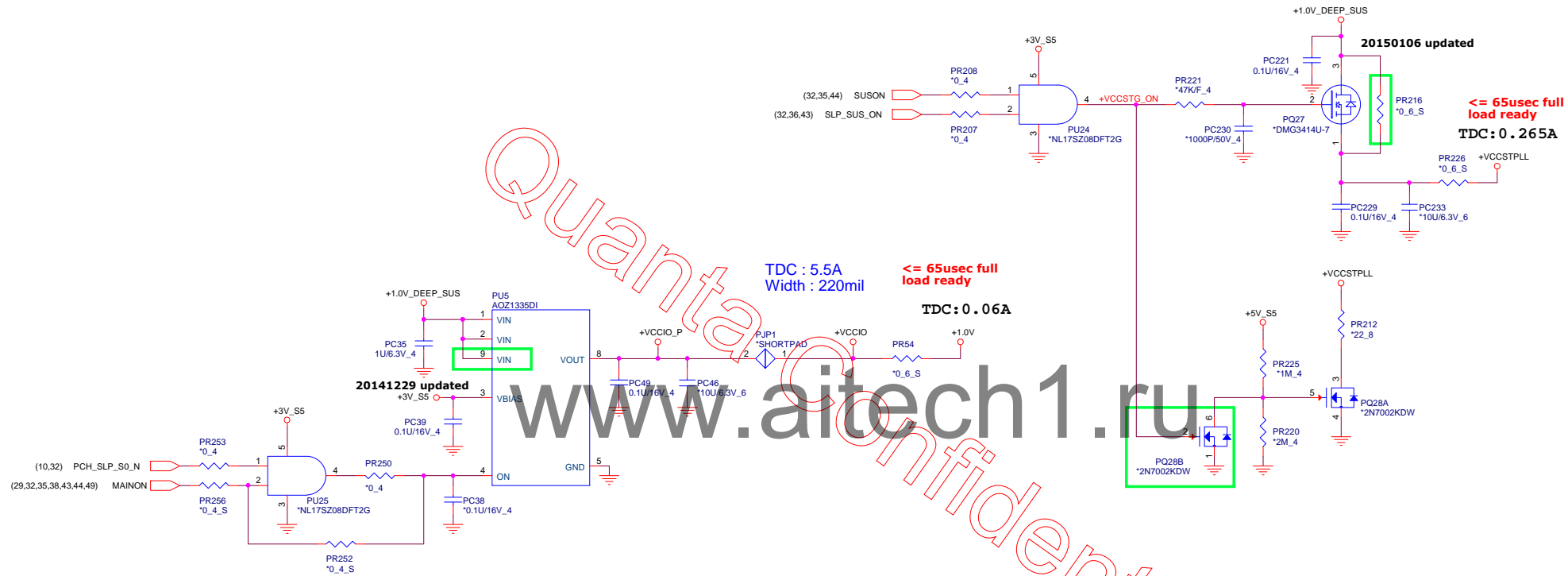


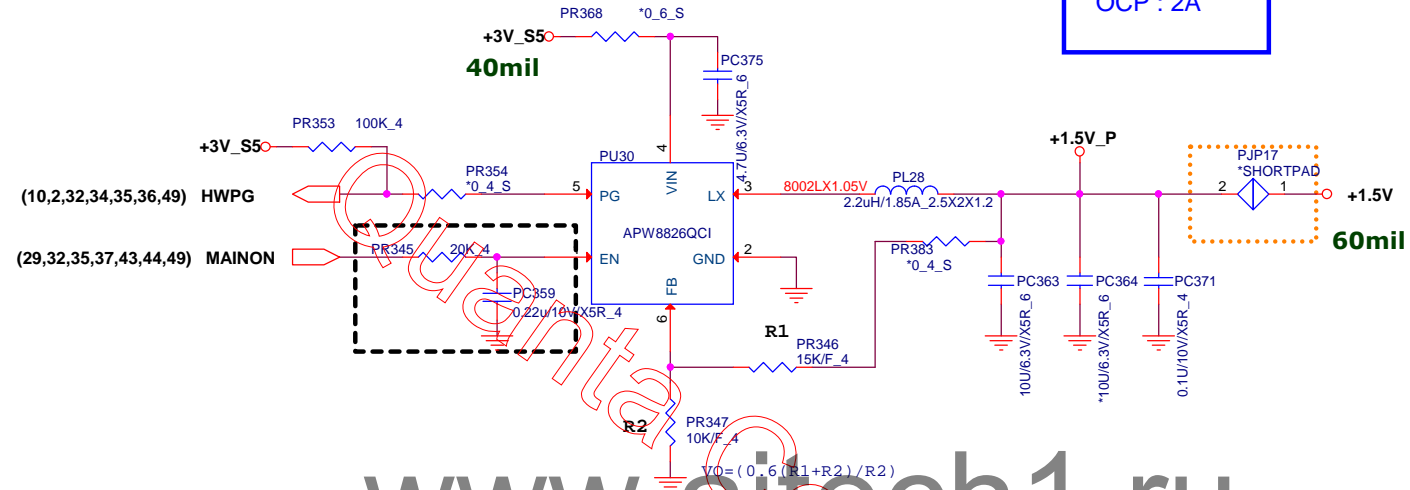
Quanta Computer Inc.

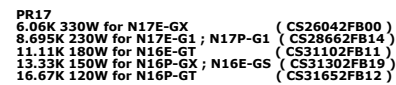
PROJECT : NL8E

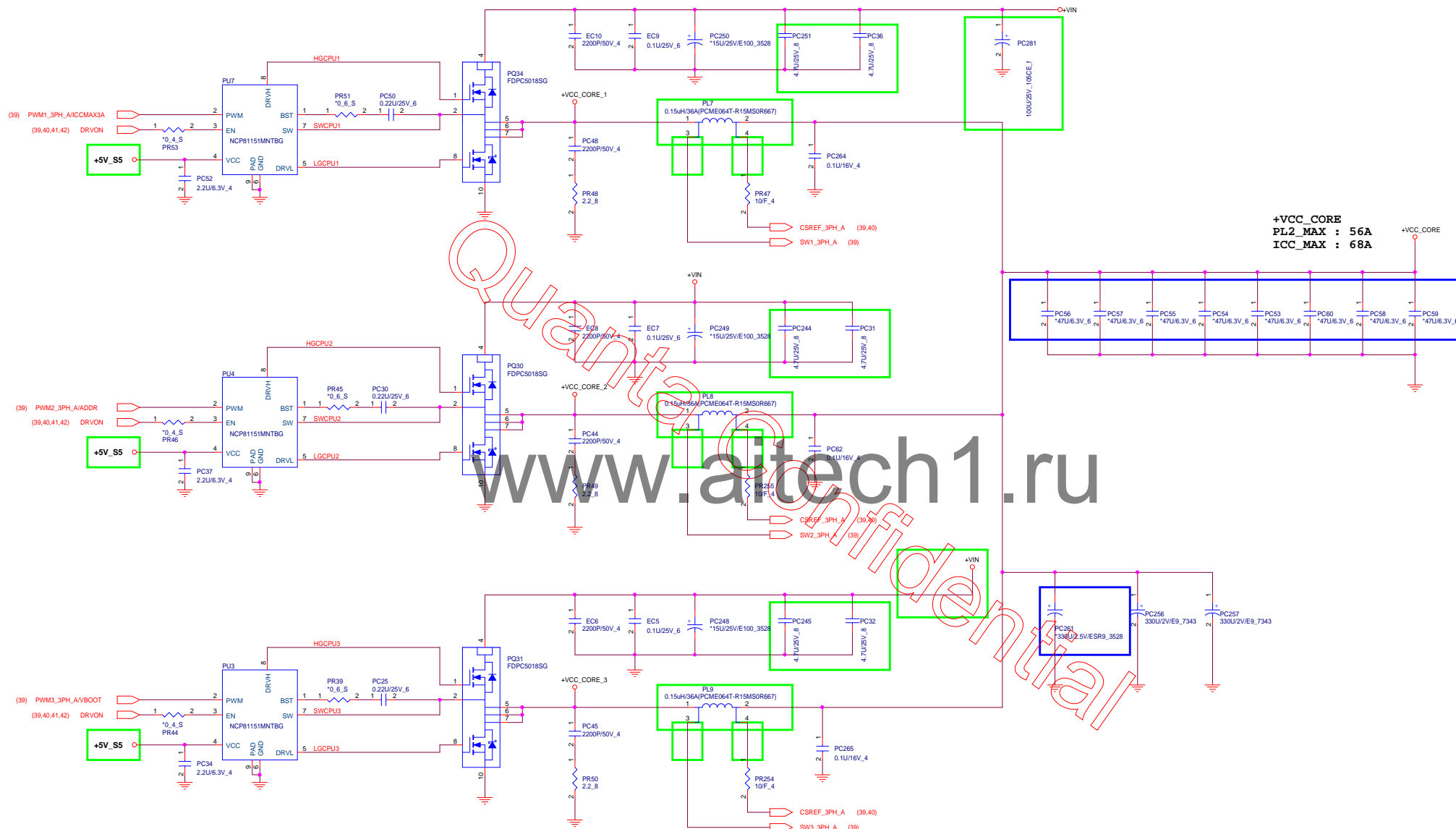
Size	Document Number	Rev
	+1V_S5 (RT8237CZQW)	1A
Date:	Thursday, August 25, 2016	Sheet 36 of 68

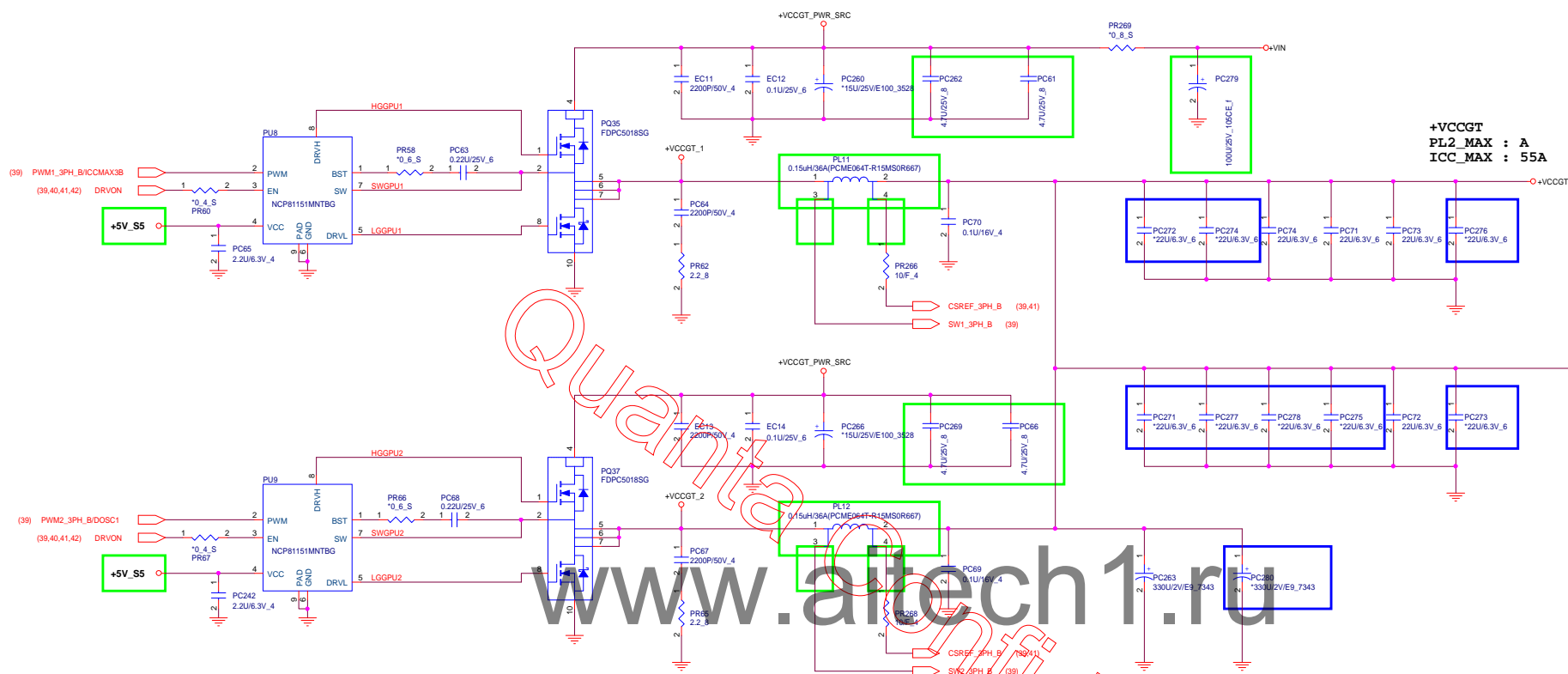
+1.0V (10,2,32,6)
 +3V_S5 (10,12,14,21,23,25,26,27,28,31,32,34,38,39,43,49,52)
 +5V_S5 (10,26,28,29,34,35,36,39,40,41,42,43,44,45,46,47,49,50,51,52)
 +VCCIO (3,6)
 +VCCSTPLL (11,2,6)
 +1.0V_DEEP_SUS (10,11,14,36,39,44)



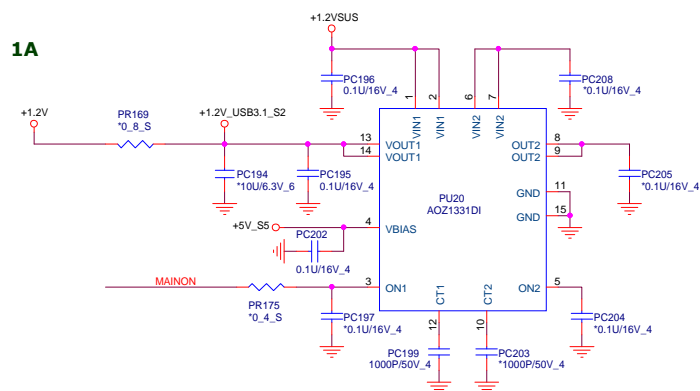
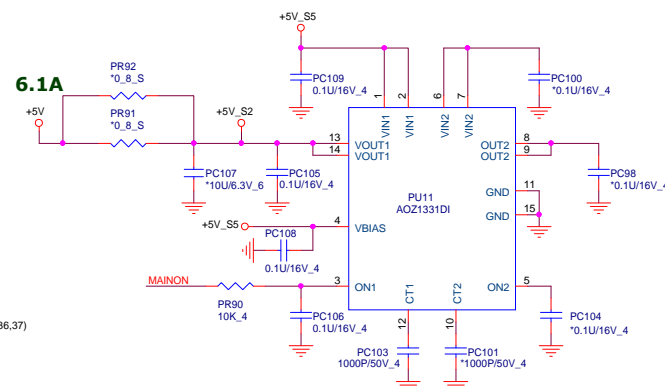






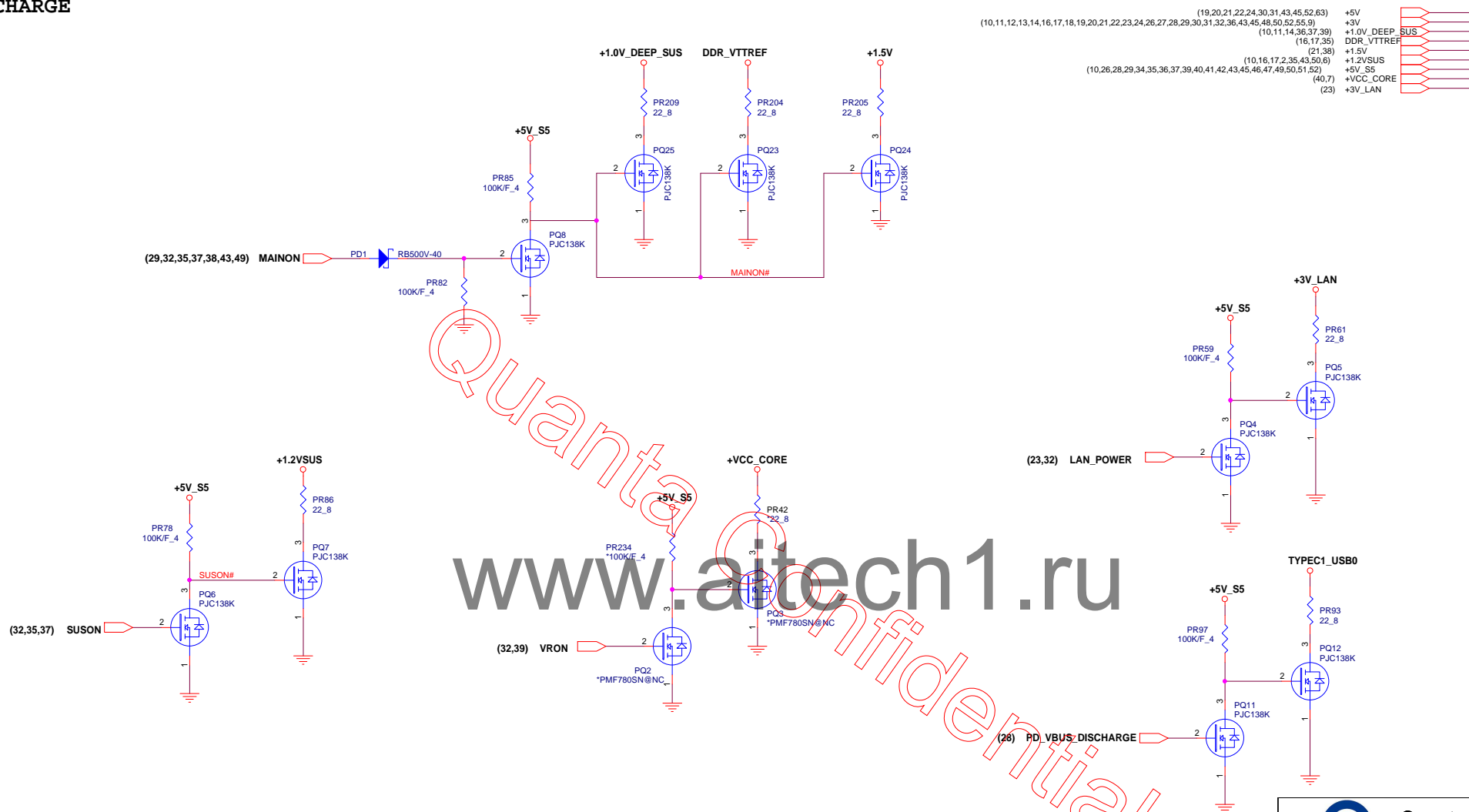







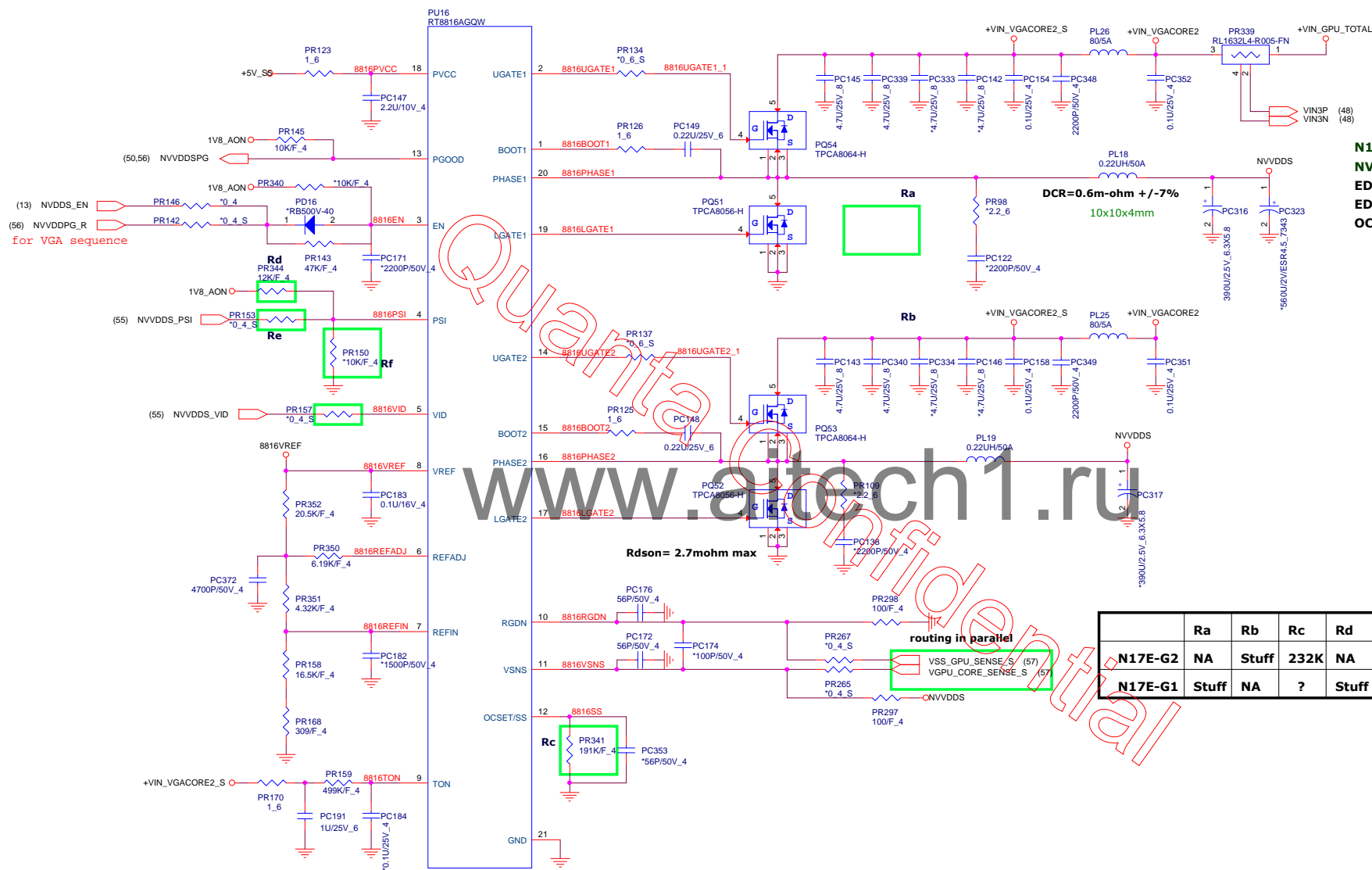
DISCHARGE

47




 Quanta Computer Inc. PROJECT :		Rev 3B
Size Custom	Document Number	
Date:	Sheet	44 of 66
Thursday, August 25, 2016		





N17E-G1
NVDDS
EDP: 18A
EDP: peak: 30.7A
OCP minimum: 63A

	Ra	Rb	Rc	Rd	Re	Rf
N17E-G2	NA	Stuff	232K	NA	Stuff	NA
N17E-G1	Stuff	NA	?	Stuff	NA	Stu



 +3V (10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,48,50,52,55,9)
 +VIN (18,33,34,35,36,39,40,41,42,47,50,52,63)
 +5V_S5 (10,26,28,29,34,35,36,37,39,40,41,42,43,44,45,47,49,50,51,52)
 NVVDDS (51,57)
 1V8_AON (19,20,45,47,49,50,53,55,56,9)

9xxx

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.55V
0	1.35V

FBVDDQ_MEM
N17E-G1
EDP: 19.8A
EDP: peak: 32.2A
OCF minimum: 64A

+VIN (18,33,34,35,36,39,40,41,42,50,52,63)
+5V_S5 (10,28,29,34,35,36,37,39,40,41,42,43,44,45,46,49,50,51,52)
FBVDDQ_MEM (51,55,54,56,58,59,60)



Quanta Computer Inc.

PROJECT :
+1.35V_GFX (AOZ2263QI-18)

Size

Document Number
Custom

Date

Rev

68

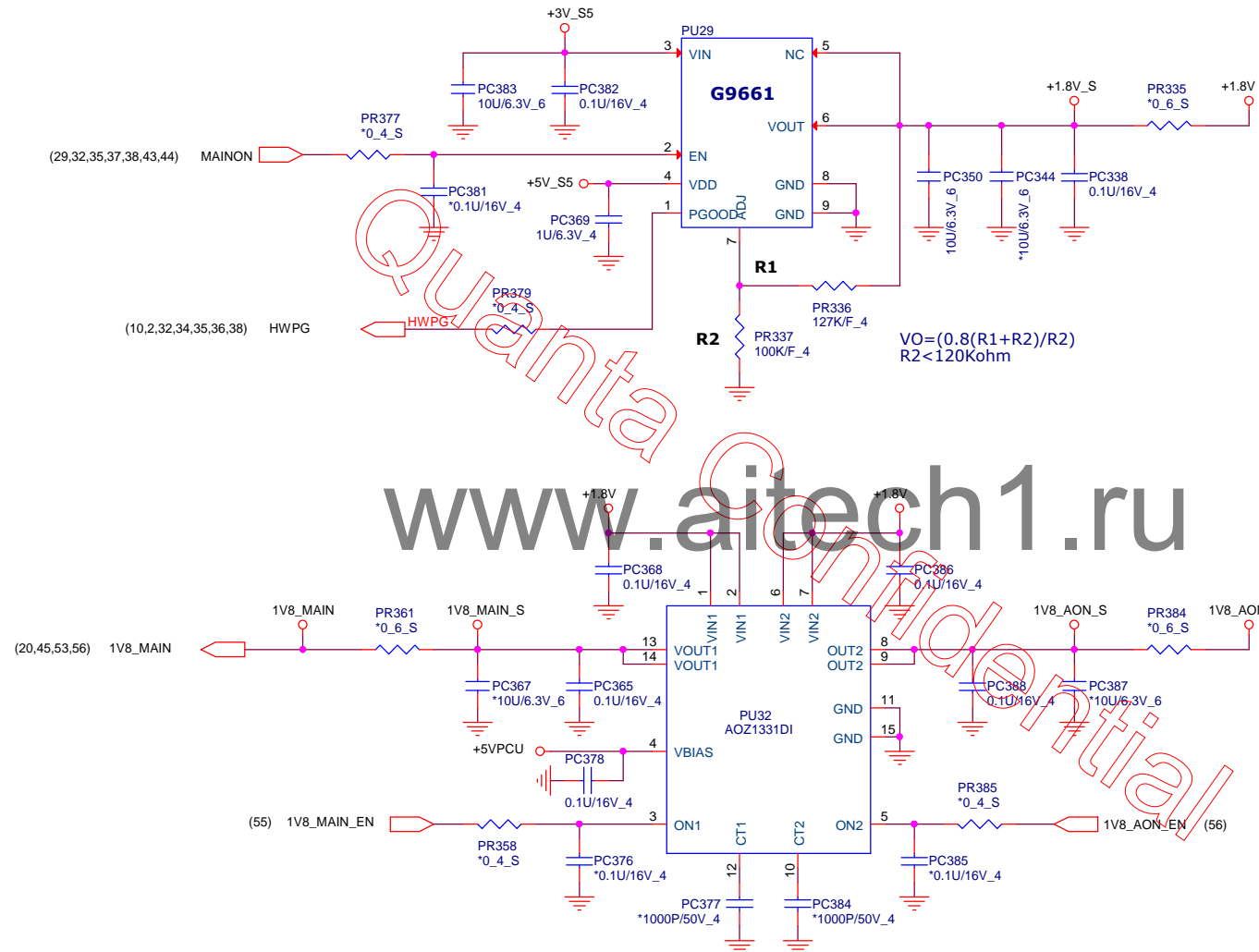
Thursday, August 25, 2016

68



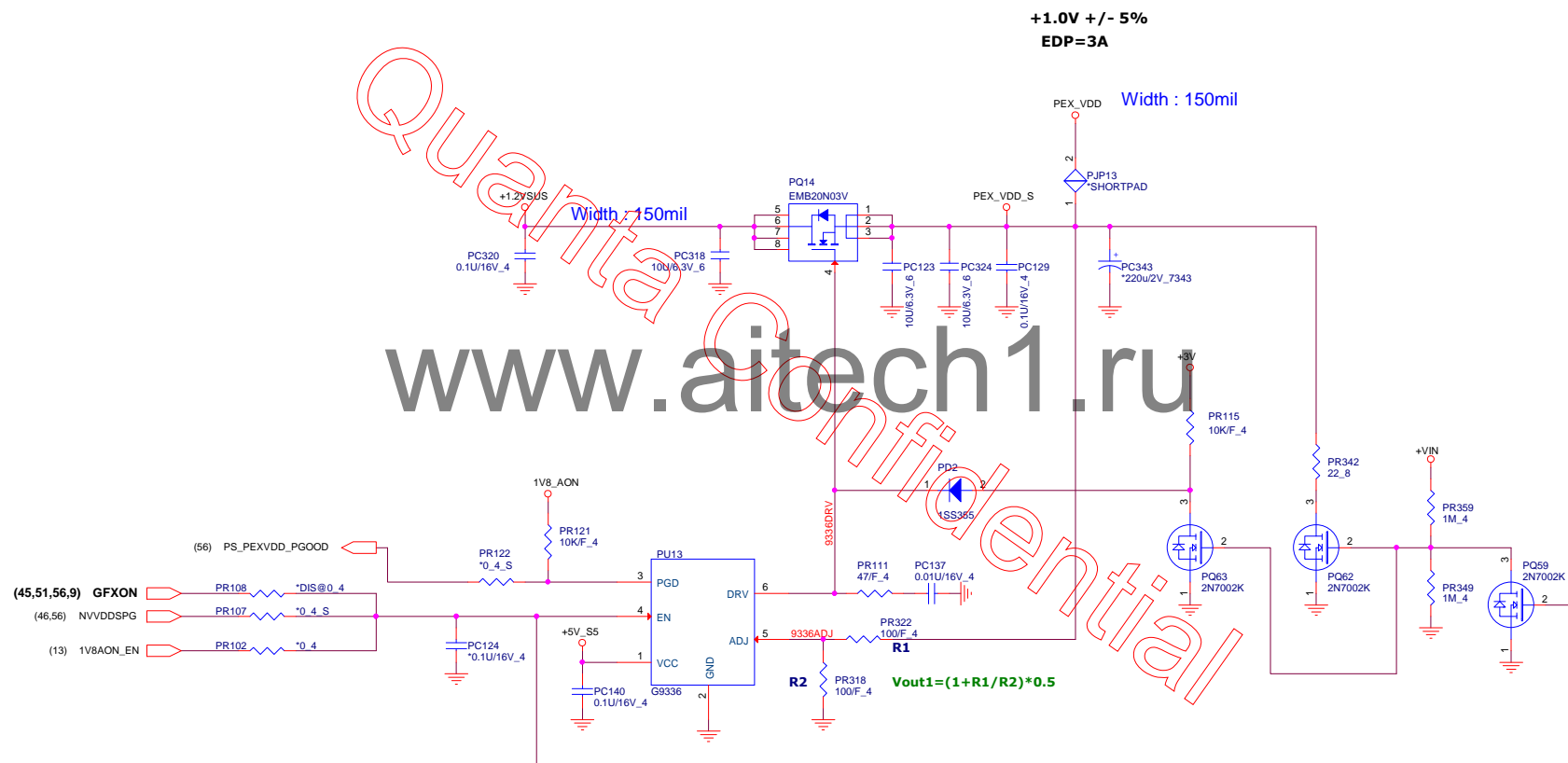


+1.8V +/- 5%
TDC:1A
PACK:2A

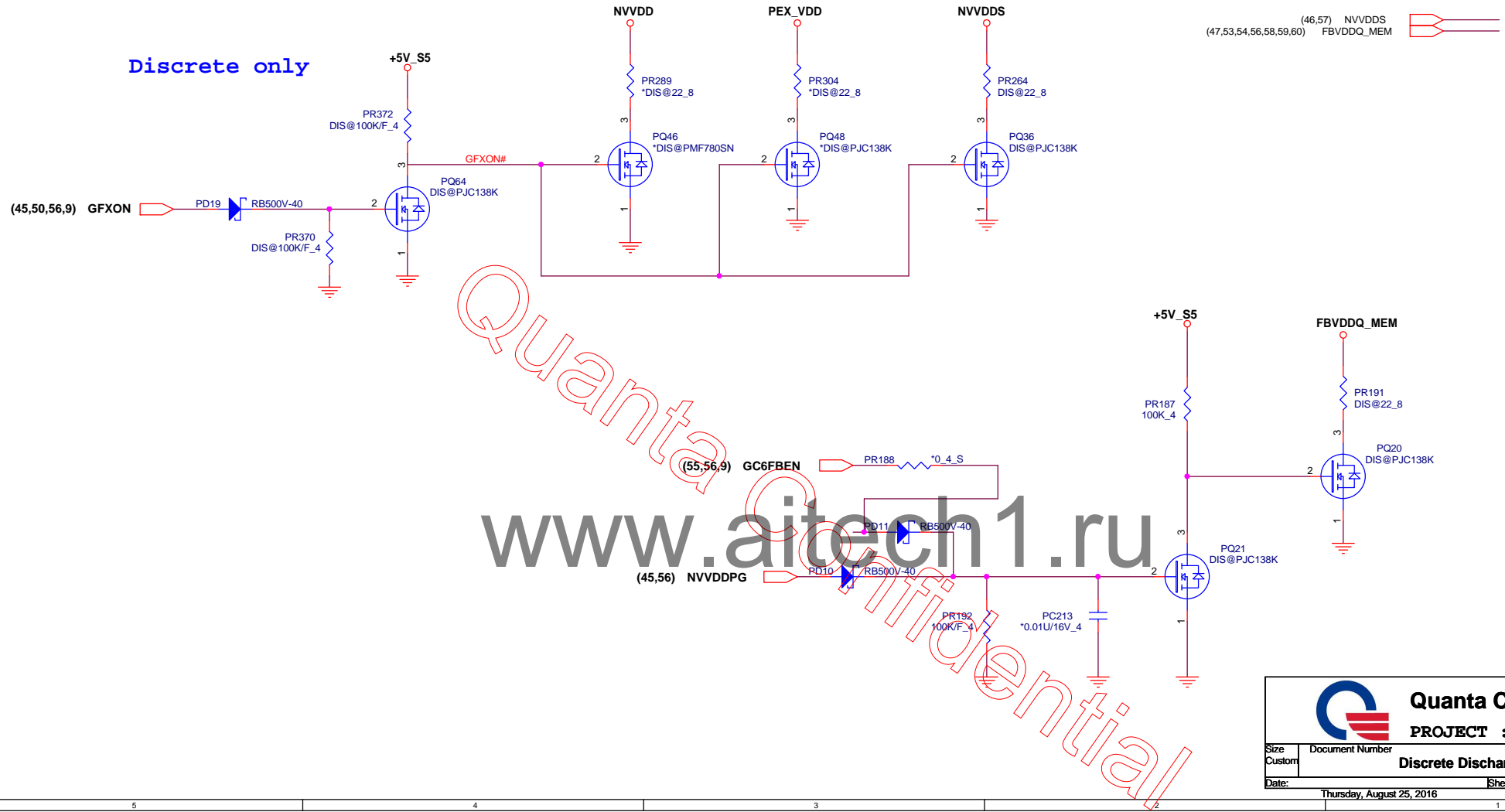



+VIN (18,33,34,35,36,39,40,41,42,47,52,63)
 +3V_S5 (10,12,14,21,23,25,26,27,28,31,32,34,37,38,39,43,49,52)
 +5V_S5 (10,26,28,29,34,35,36,37,39,40,41,42,43,44,45,46,47,49,51,52)

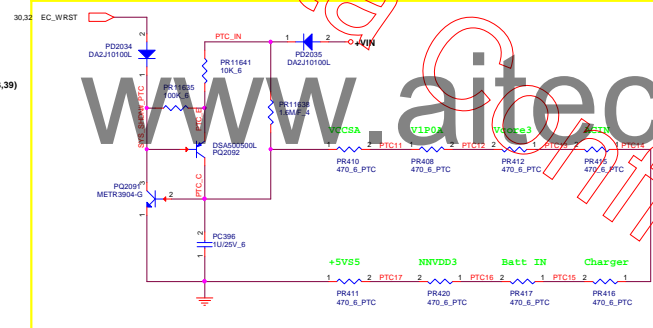
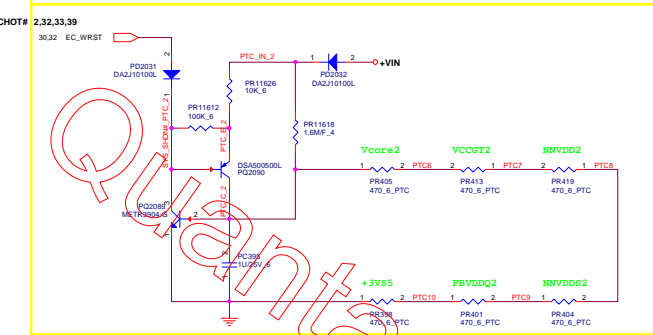
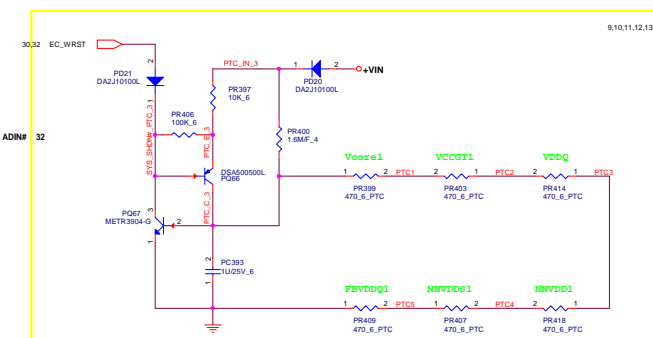
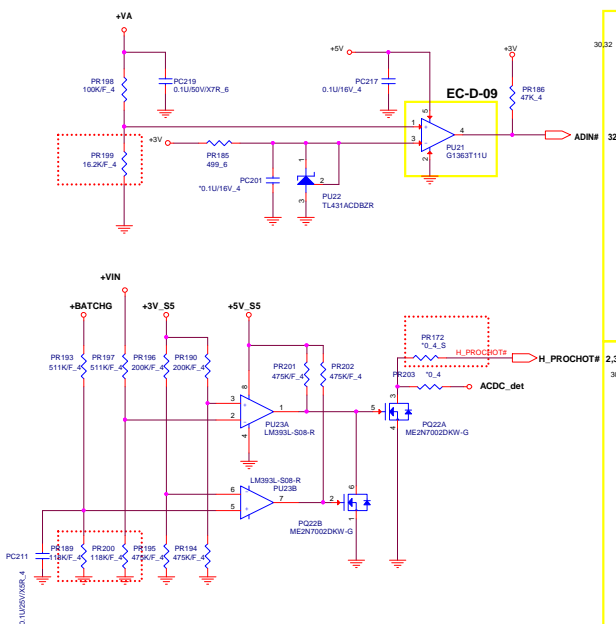
+1.2VSUS (10,16,17,2,35,43,44,6)
 PEX_VDD (51,53,55)



Discrete only

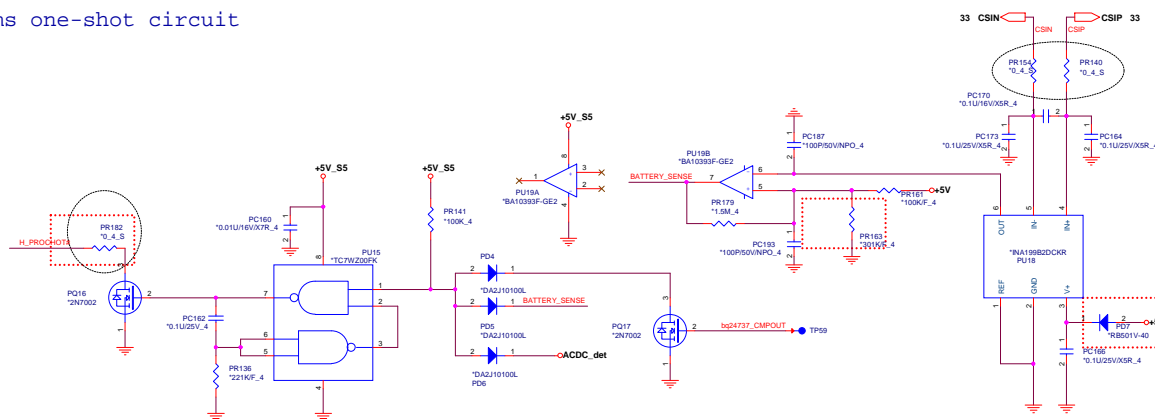


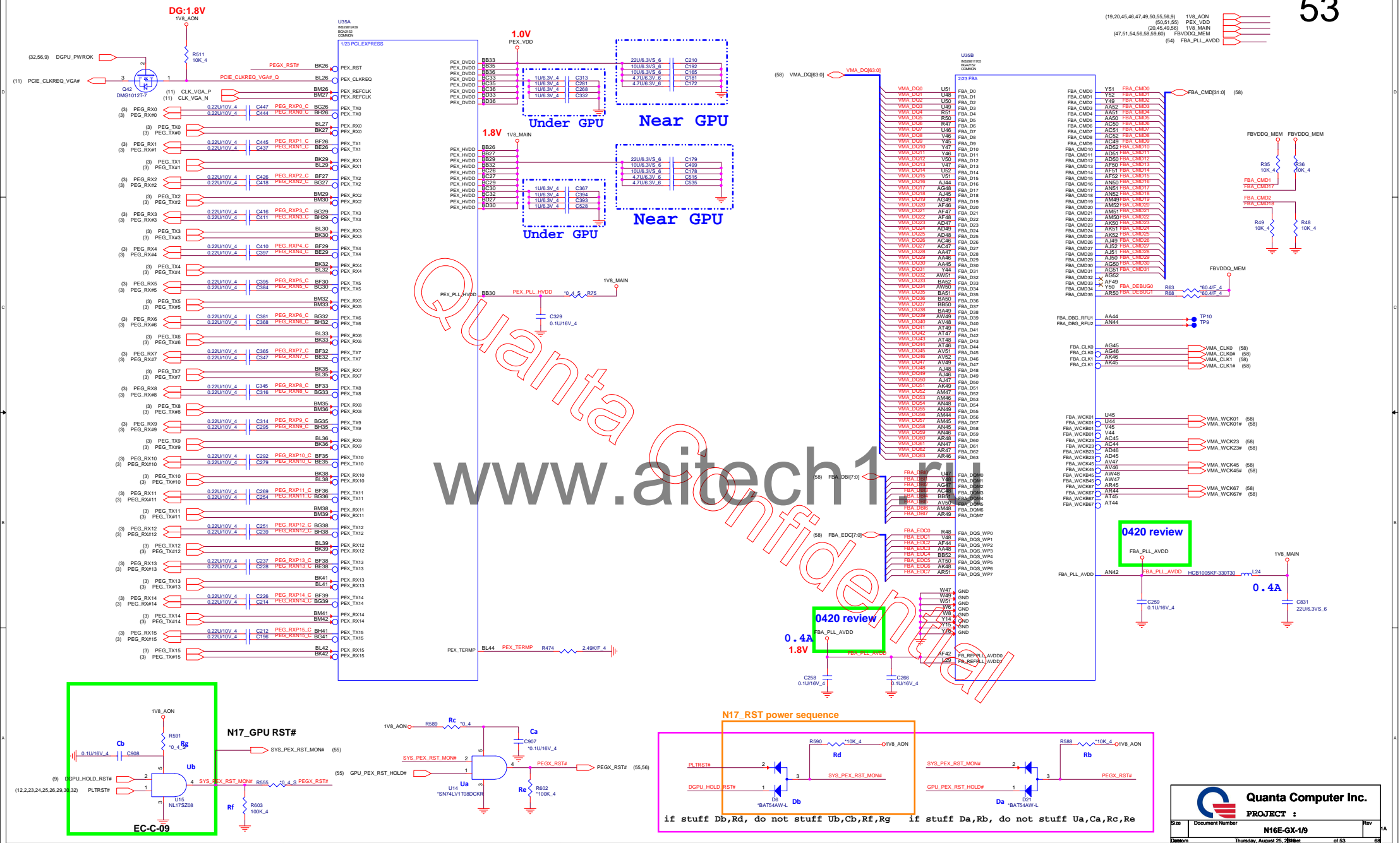
 Quanta Computer Inc.	
PROJECT :	
Size Custom	Document Number
Discrete Discharge	
Date:	Rev 38
Thursday, August 25, 2016	
Sheet 51	of 66

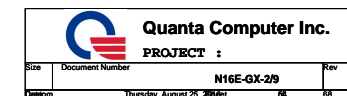


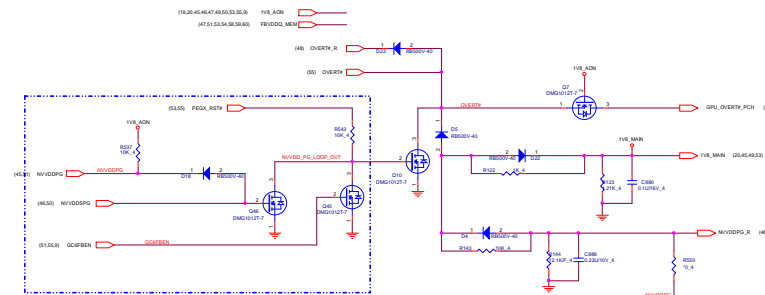
www.aitech1.ru

10ms one-shot circuit

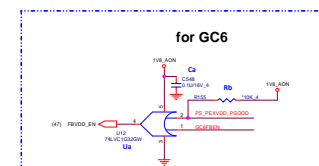




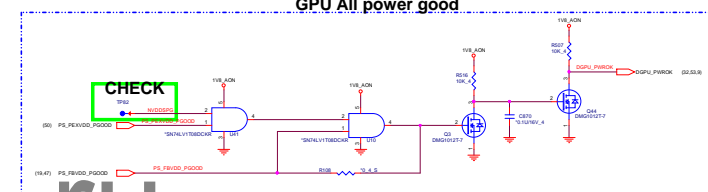




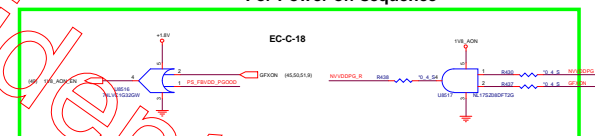
Overt temp ckt for NVVDD and NVVDDS

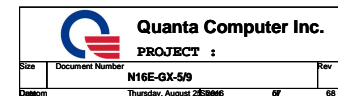


GPU All power good



For Power off sequence





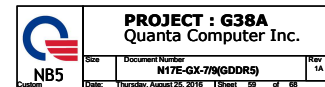
FBVDDQ_MEM

MF=0 Non-mirrored



Channel 0
<0-31>

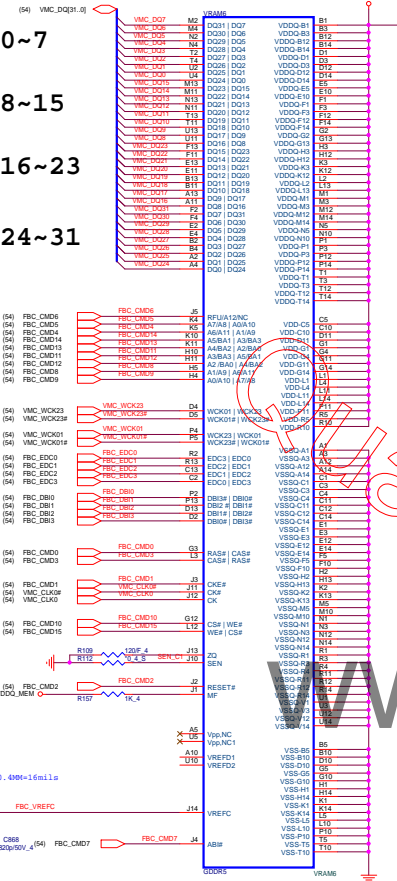
MF=0 Non-mirrored



Channel 0
<0-31>

MF=0 Non-mirrored

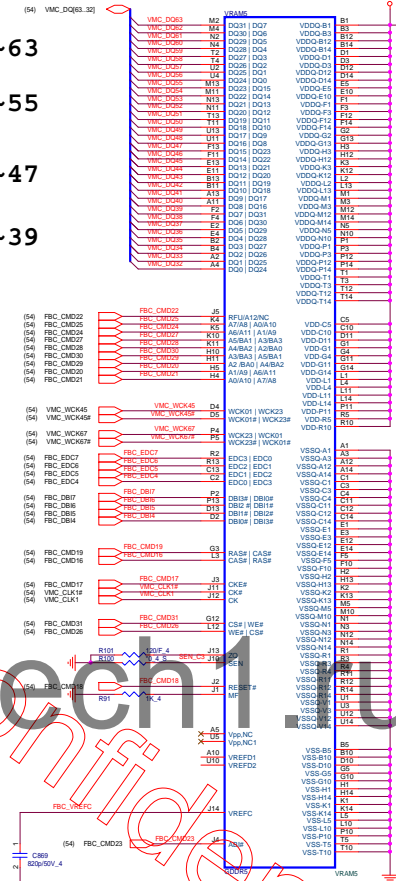
QD0~7
QD8~15
QD16~23
QD24~31



Channel 1
<0-31>

MF=0 Non-mirrored

QD56~63
QD48~55
QD40~47
QD32~39



(47.51,53,54,56,58,59)

FBVDDQ_MEM

Table 7-5. GDDR5 Mode F Mapping


GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	AB*	CMD23	AB*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	C5*	CMD31	C5*
GB3-256 Channel 0 & 1			
CMD32	Hot used		
CMD33	Hot used		
CMD34	DEBUG		
CMD35	DEBUG		

Notes:

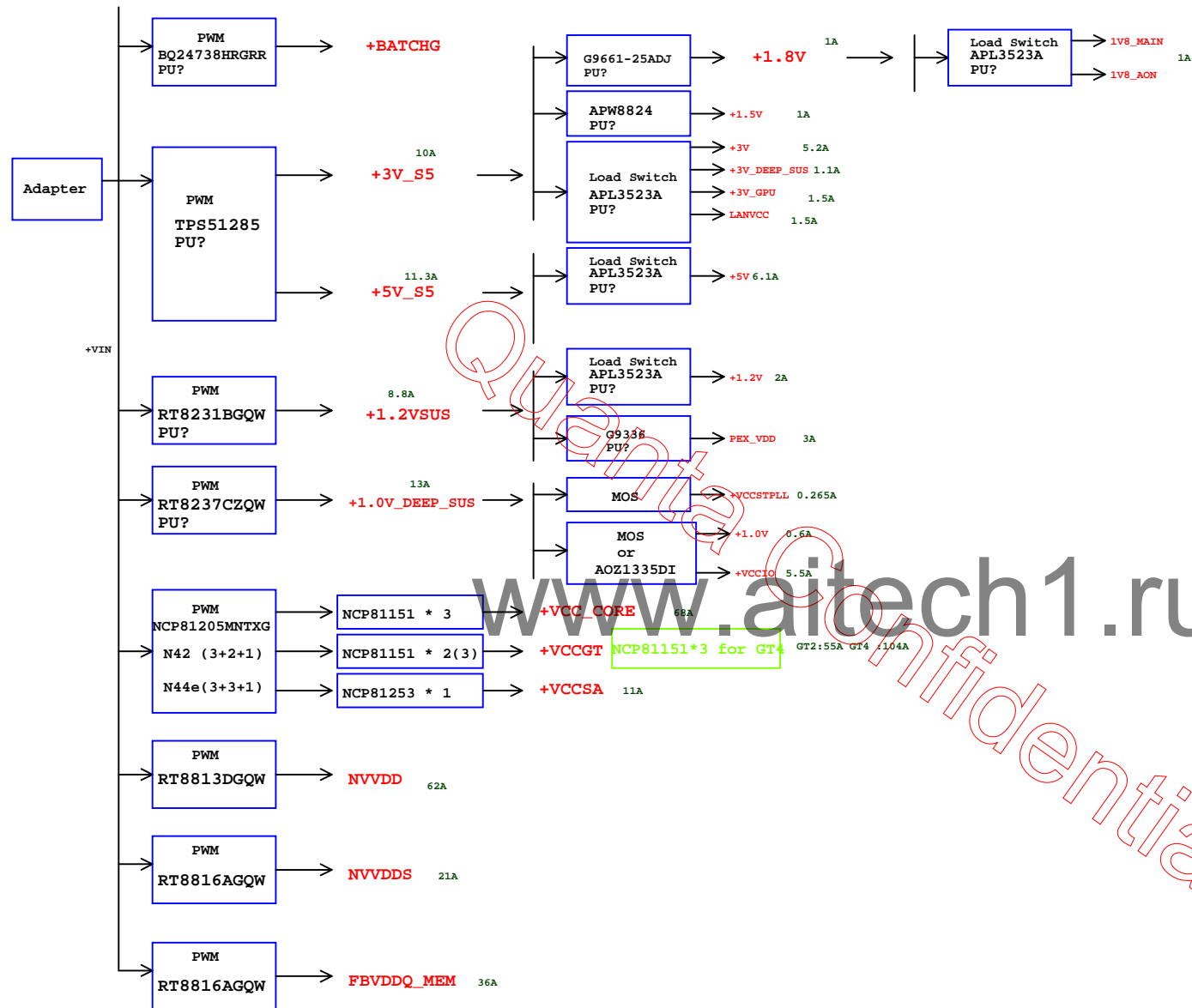
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

Quanta Confidential

www.aitech1.ru

 Quanta Computer Inc. PROJECT :		Rev
		3B
Size Custom	Document Number blank	
Date: Thursday, August 25, 2016	Sheet 61	of 68

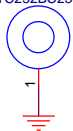
Power Delivery Map



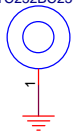


CPU BRACKET

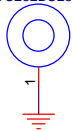
H11
*H-TC252BC236D150P2



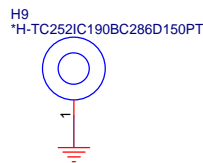
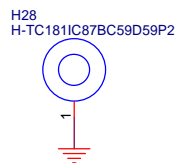
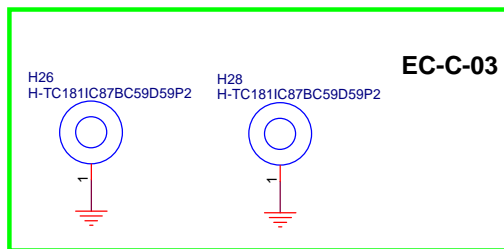
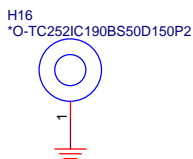
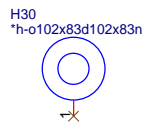
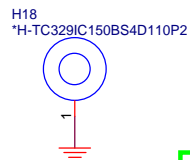
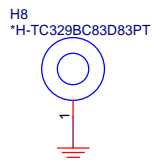
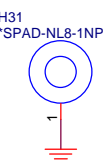
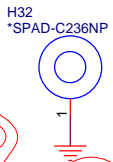
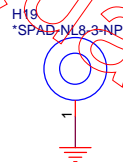
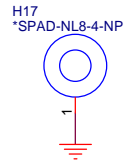
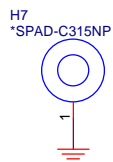
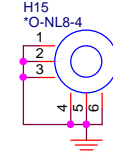
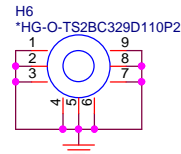
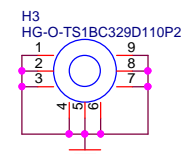
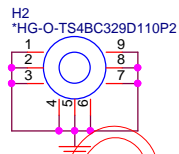
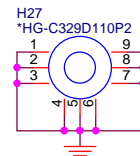
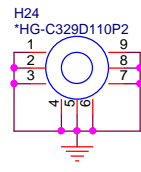
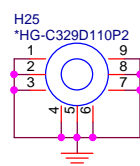
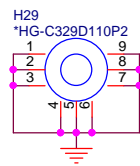
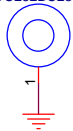
H13
*H-TC252BC236D150P2



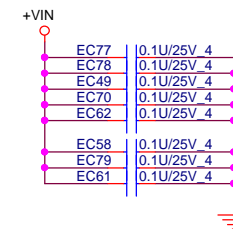
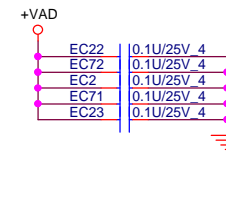
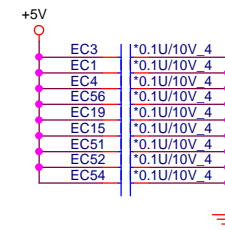
H14
*H-TC252BC236D150P2



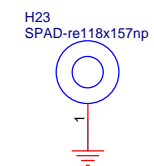
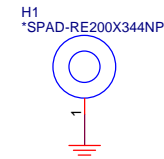
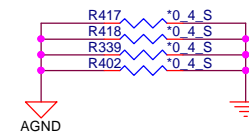
H12
*H-TC252BC236D170X150P2



EMI



ESD



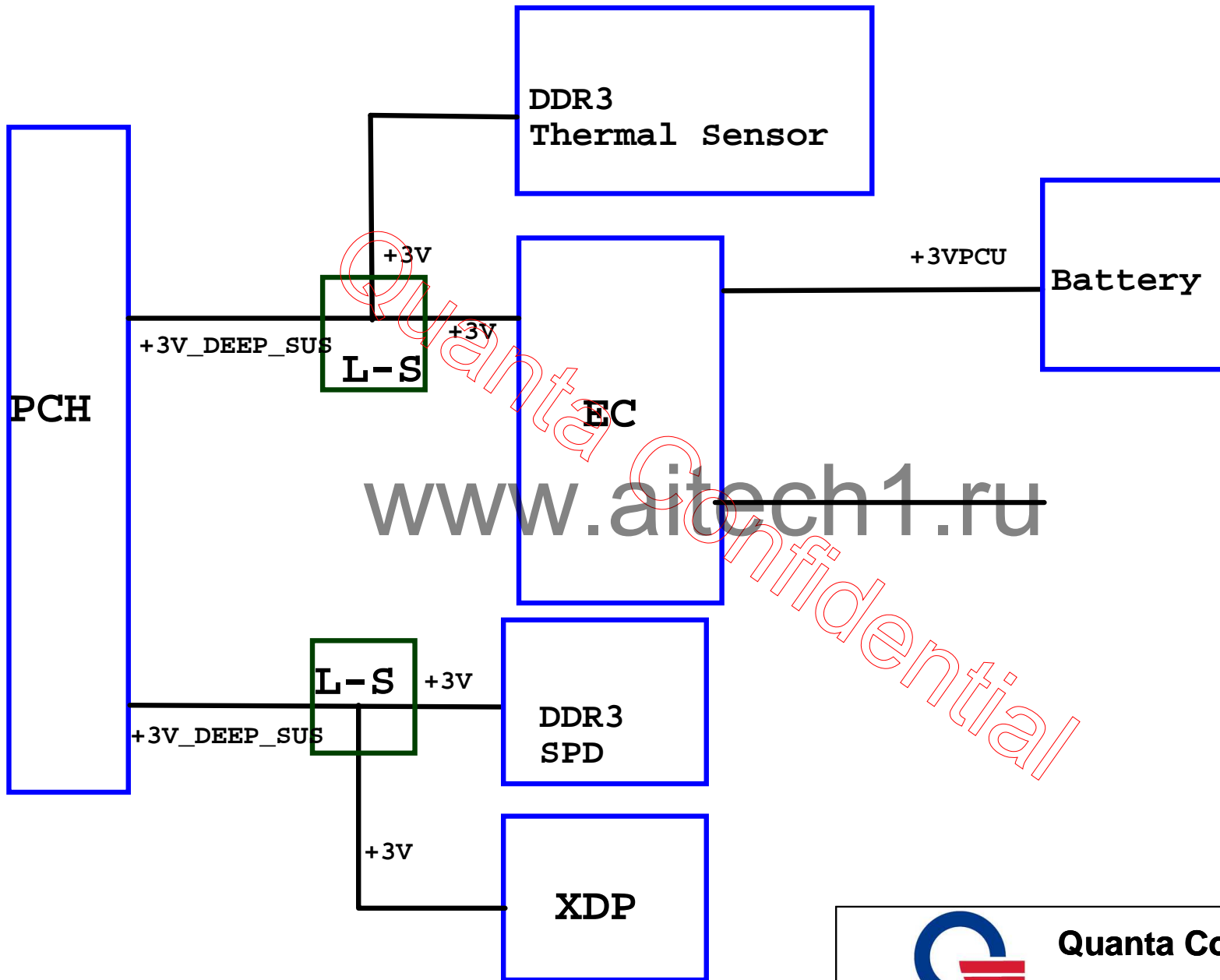
www.aitech1.ru

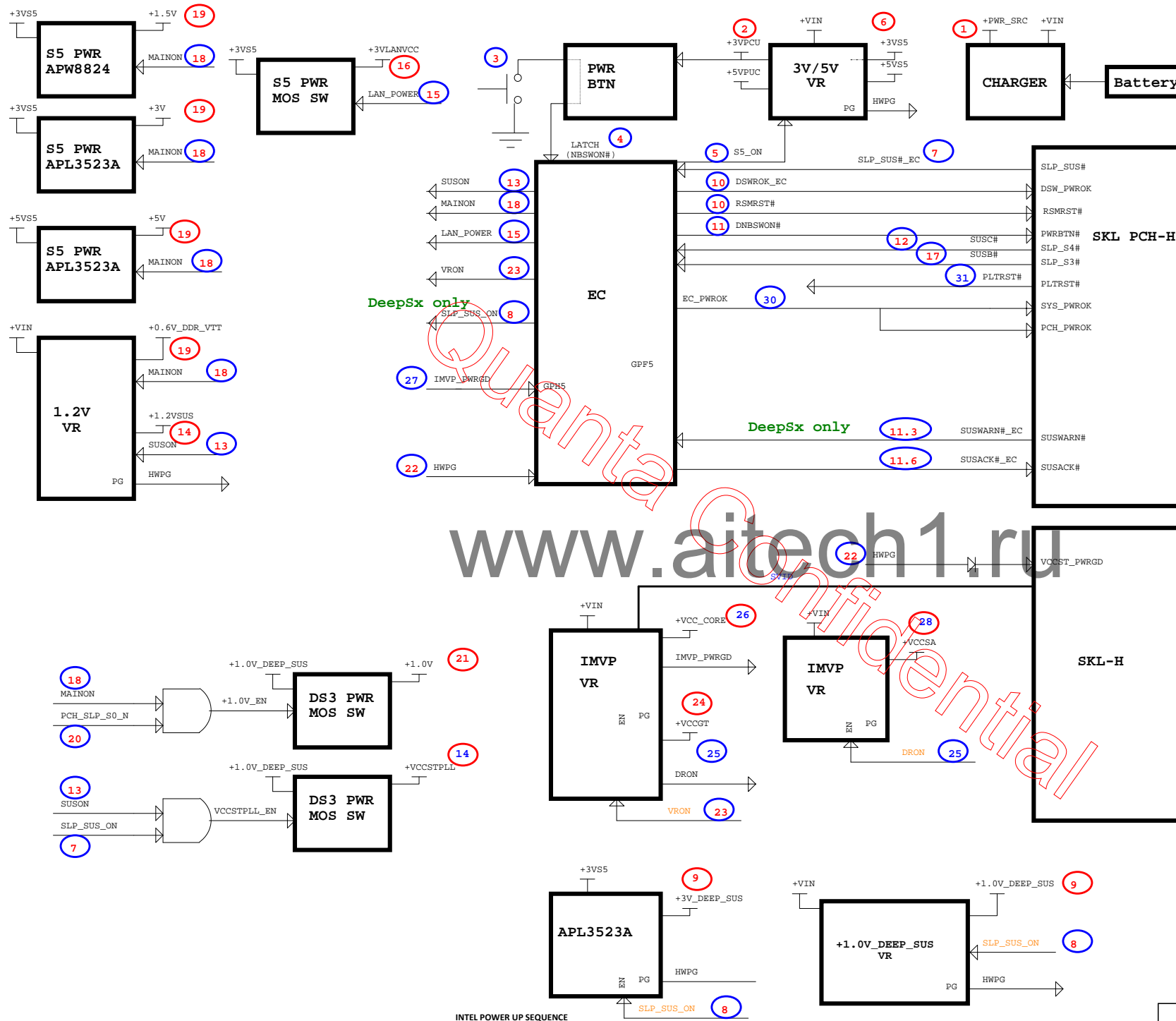


Quanta Computer Inc.

PROJECT :

Size Custom	Document Number HOLE	Rev 3B
Date:	Thursday, August 25, 2016	Sheet 63 of 68





www.aitech1.ru

2015

B

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-B-01	55,58,59,60			VRAM change to right PN
EC-B-02			R246 NC (sortpad)	schematic value error
EC-B-03	55		add R745, NC R556	NV update
EC-B-04				SSD WLAN (CN16&CN15)change FP add -smt
EC-B-05	22		R759 ASM	for speaker no function issue
EC-B-06	20		Del U28,R424,R423,R432,C761,C757,C741,C742,C762 Add R749 R747 Q57 Q58 Q56 R746 R750 r751 R752 R753 R754R755 R756 R7598 R760 C1043 Q59 Q61 R462 R763 C1046 c1047 c1048 c1049 c741 R432	HDMI change to GPU output for VR
EC-B-07	21		C992	wrong FP ,update to 0402
EC-B-08	10		Add R761 R757 R424 R423	change to chargeable RTC
EC-B-09	29		Add C1044 C1045 ,CN13 change to 50pin	change USB2 to USB3 for update SPEC
EC-B-10	9		Add R719 R427	GDPU power GPIO update@PCH for voltage level
EC-B-11			Add C1050 C1051 C1052 C1053 C742 R433 R764 R765 R768 R769 R767 R766 R762 Del U29 C769 C755 R430 D16 L22 R10 R9 R8 L2 R3 R4 R440 R439 R436 R438 D2 C6 L21 L3 L1 C753 C9 C8 C7 C10 C749 CN4 C9 C4	remove CRT function, add miniDP and change to GPU output
EC-B-12				BAM34130001change FP for SMT request
EC-B-13			Del R11 R12 R13 R19 C765 R443 U30	change RJ45 conn w/ transformer
EC-B-14			U39	change GPU EEPROM to 150mil
EC-B-15			Add R435	
EC-B-16			Add U53,del U54	BIOS change socket to rom for B test
EC-B-17	19		R8595 change to GND	INT_DP_AUXP switch change connection
EC-B-18	55		Add C1056, C1057	display change to GPU output
EC-B-19	9		R714 10k stuff	display change to GPU output

EC-B-20 19

Add R12170, R12171, R12172, R12173, Q7744, Q7745, Q7746, Q7747 For old NVidia G-SYNC monitor (R1 version)

EC-B-21 20

change R746, R750, R751, R752, R753, R754, R755, R756 including the R2 version /0614

EC-B-22 19

Add Q7749, R12178, R12179, R12180, R12181, Q7752

change HDMI_HPDP & DP_HPDP are low active



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
Date	Thursday, August 25, 2016	66 of 68

EC list-1

Sheet 66 of 68

EC-C-01	add R436 R768 , NC R167	for type C HPD
EC-C-02	C604,C943,C944	change 0402 correct PN
EC-C-03	ASM H26 H28,NC EC63	
EC-C-04	remove C778(NC)	for DCIN plug of space
EC-C-05	R162 R170	cypress recommond change to 200Kohm
EC-C-06	Q24 Q15 Q39 Q37	change FP for SMT
EC-C-07	C649	change cap for vendor recommend
EC-C-08	R629 ASM, R628 NC	we use cable detect ,NL8C cable pin6 gnd =low, NL9 cable pin6 NC NL9 have ext PU (R629)=high
EC-C-09	U15	change PN for 2nd source team recommend
EC-C-10	CN6 camera	change to Vertical type &FP
EC-C-11	CN1 typeC	change to type-C FP
EC-C-12	Y2	change to 3225 size for buyr recommond
EC-C-13	R427 ASM ,del Q54 , add R771 ,Q61,Q62	change GC6EN circuit
EC-C-14	R772 R769	NV review
EC-C-15		CORE_PLLVDD power rail
EC-C-16	Del R430,Q7749 Add R12183 R12184 Q7762	NV recommed
EC-C-17	C649	change cap for vendor recommend
EC-C-18	U8516 U8517 ASM	GPU power down sequence

Title <Title>		
Size B	Document Number <Doc>	Rev <RevCode>
Date:	Thursday, August 25, 2016	Sheet 67 of 68

A vertical bar divided into four segments labeled A, B, C, and D from bottom to top. An arrow points from the boundary between B and C to the right.